AMENDED APPEAL BRIEF

In RE United States Patent Application of

Taeg-Hyun Kang
Jun-Hyeong Ryu and
Jong-Hwan Kim

Serial Number

10/071,494

Filed

February 6, 2002

Titled

Field Transistors for Electrostatic Discharge Protection and Methods for Fabricating the Same

---

Examiner: Victor A. Mandala, Jr.

Art Unit: 2826

TABLE OF CONTENTS

REAL PARTY IN INTEREST

The real party in interest in the present Appeal is the assignee of record, Fairchild Korea Semiconductor, Ltd., by virtue of two Assignments from the inventors to Fairchild Semiconductor Corporation and then from that entity to Fairchild Korea Semiconductor, Ltd.

RELATED APPEALS AND INTERFERENCES

None, to the best of undersigned's knowledge.

STATUS OF CLAIMS

Claims 1-41 are pending in the application.

Claims 11-18 and 30-39 withdrawn from consideration as being directed to a non-elected invention.

Claims 1-10, 19-29, and 40-41 stand rejected.

The rejection of claims 1-10, 19-29, and 40-41 is being appealed.

STATUS OF AMENDMENTS

Applicants submitted a Request for Reconsideration that included no amendments to the claims. The Request for Reconsideration contained arguments directed to the rejections and contained a declaration under 37 C.F.R. § 1.132 on June 28, 2005. In response to the Request for Reconsideration, the Examiner denied entry of the declaration under § 1.132 and found the arguments non-persuasive.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent Claim 1. Claim 1 recites a field transistor (illustrated in Figure 2 and described in paragraphs [13] (all paragraph numbers herein refer to the numbering provided by Applicants in the specification as filed) and [27]-[29]) having a current path between a source and a drain (paragraph [32]) while containing no thin gate insulating layer 19 such as contained in the prior art (see Figure 1, paragraph [08]). The claimed transistor includes a well region 130 (paragraph [13] lines 1-2, paragraph [28] line 2) of a first conductivity type, a field oxide layer 170 (paragraph [13] lines 2-3, paragraph [30] lines 8-13) for defining an active region on the well region 130, a high concentration source region 140 (paragraph [13] lines 3-4, paragraph [28] lines 9-11) of a second conductivity type, and a high concentration drain region 150 (paragraph [13] lines 3-4, paragraph [28] lines 9-11) of a second conductivity type where the source region 140 and drain region 150 are separated from each other by a width of the field oxide layer 170 (paragraph [13] lines 3-4, paragraph [28] lines 9-11). The claimed transistor also includes a low concentration source region 145 of the second conductivity type formed in the well region 130 adjacent to the high concentration source region 140 and overlapped by one end of the field oxide layer 170 (paragraph [13] lines 4-7, paragraph [29] lines 1-6) and a low concentration drain region 155 of the second conductivity type formed in the well region 130 adjacent to the high concentration drain region 150 and overlapped by the other end of the field oxide layer 170 (paragraph [13] lines 7-10, paragraph [29] lines 1-6). The claimed transistor finally requires a gate conductive layer pattern 180 formed on the field oxide layer 170 to overlap parts of the low concentration source region 145 and the low concentration drain region 155 (paragraph 13 lines 10-12, paragraph [31] lines 1-5).

Independent claim 19. Claim 19 recites a semiconductor device (illustrated in Figure 2 and described in paragraphs [13] and [27]-[29]) having a current path between a source and a drain (paragraph [32]) while containing no thin gate insulating layer 19 (see Figure 1, paragraph [08]). The claimed device includes a substrate 110 (paragraph [28] line 2) comprising a well region 130 (paragraph [13] lines 1-2, paragraph [28] line 2) of a first conductivity type, a field oxide layer 170 (paragraph [13] lines 2-3, paragraph [30] lines 8-13) located over a portion of the well region 130, a first source region 140 (paragraph [13] lines 3-4, paragraph [28] lines 9-11) of a second conductivity type, and a first drain region 150 (paragraph [13] lines 3-4, paragraph [28] lines 9-11) of a second conductivity type separated from the first source region 140 by the field oxide layer 170 (paragraph [13] lines 3-4, paragraph [28] lines 9-11). The claimed device also includes a second source region 145 having a second conductivity type concentration lower than the first source region 140, being formed in the well region 130 adjacent to the first source region 140, and having a portion underlying the field oxide layer 170 (paragraph [13] lines 4-7, paragraph [29] lines 1-6) and a second drain region 155 having a second conductivity type concentration lower than the first drain region 150, being formed in the well region 130 adjacent to the first drain region 150, and having a portion underlying the field oxide layer 170 (paragraph [13] lines 7-10, paragraph [29] lines 1-6). The claimed device finally requires a conductive layer 180 formed over the field oxide layer 170 and overlapping the second source region 145 and the second drain region 155 (paragraph 13 lines 10-12, paragraph [31] lines 1-5).

Independent Claim 27. Claim 27 recites a semiconductor device (illustrated in Figure 2 and described in paragraphs [13], [16], [27]-[29], and [31]) having a current path between a source and a drain (paragraph [32]) while containing no thin gate insulating layer 19 (see Figure 1, paragraph [08]). The claimed device includes a substrate 110 (paragraph [28] line 2)

comprising a well region 130 (paragraph [13] lines 1-2, paragraph [28] line 2) of a first conductivity type, a field oxide layer 170 (paragraph [13] lines 2-3, paragraph [30] lines 8-13) located over the well region 130, a first source region 140 (paragraph [13] lines 3-4, paragraph [28] lines 9-11) of a second conductivity type, and a first drain region 150 (paragraph [13] lines 3-4, paragraph [28] lines 9-11) of a second conductivity type separated from the first source region 140 by the field oxide layer 170 (paragraph [13] lines 3-4, paragraph [28] lines 9-11). The claimed device also includes a second source region 145 having a second conductivity type concentration lower than the first source region 140, being formed in the well region 130 adjacent to the first source region 140, and having a portion underlying the field oxide layer 170 (paragraph [13] lines 4-7, paragraph [29] lines 1-6) and a second drain region 155 having a second conductivity type concentration lower than the first drain region 150, being formed in the well region 130 adjacent to the first drain region 150, and having a portion underlying the field oxide layer 170 (paragraph [13] lines 7-10, paragraph [29] lines 1-6). The claimed device also requires a conductive layer 180 formed over the field oxide layer 170 and overlapping the second source region 145 and the second drain region 155 (paragraph 13 lines 10-12, paragraph [31] lines 1-5). The claimed device finally requires a gate electrode 200 electrically connected to the conductive layer 180 (paragraph [16] lines 1-2, paragraph [31] lines 6-7), a source electrode 210 electrically connected to the first source region 140 (paragraph [16] lines 2-3, paragraph [31] lines 7-8), and a drain electrode 220 electrically connected to the first drain region 150 (paragraph [16] lines 4-5, paragraph [31] lines 8-11).

Independent Claim 29. Claim 29 recites a system for electrostatic discharge protection containing a field transistor (illustrated in Figure 2 and described in paragraphs [13] and [27]-[29]) having a current path between a source and a drain (paragraph [32]) without a thin gate

insulating layer 19 (see Figure 1, paragraph [08]). The claimed transistor includes a substrate 110 (paragraph [28] line 2) comprising a well region 130 (paragraph [13] lines 1-2, paragraph [28] line 2) of a first conductivity type, a field oxide layer 170 (paragraph [13] lines 2-3, paragraph [30] lines 8-13) located over the well region 130, a first source region 140 (paragraph [13] lines 3-4, paragraph [28] lines 9-11) of a second conductivity type, and a first drain region 150 (paragraph [13] lines 3-4, paragraph [28] lines 9-11) of a second conductivity type separated from the first source region 140 by the field oxide layer 170 (paragraph [13] lines 3-4, paragraph [28] lines 9-11). The claimed device also includes a second source region 145 having a second conductivity type concentration lower than the first source region 140, being formed in the well region 130 adjacent to the first source region 140, and having a portion underlying the field oxide layer 170 (paragraph [13] lines 4-7, paragraph [29] lines 1-6) and a second drain region 155 having a second conductivity type concentration lower than the first drain region 150, being formed in the well region 130 adjacent to the first drain region 150, and having a portion underlying the field oxide layer 170 (paragraph [13] lines 7-10, paragraph [29] lines 1-6). The claimed device finally requires a conductive layer 180 formed over the field oxide layer 170 and overlapping the second source region 145 and the second drain region 155 (paragraph 13 lines 10-12, paragraph [31] lines 1-5).

Independent Claim 40. Claim 40 recites a semiconductor device for electrostatic discharge protection comprising a field transistor (illustrated in Figure 2 and described in paragraphs [13] and [27]-[29]) having a source region 140 and a drain region 150 (paragraph [13] lines3-4, paragraph [28] lines 9-11) overlapped by a gate conductive layer 180 (paragraph 13 lines 10-12, paragraph [31] lines 1-5) and having a current path between the source region

140 and the drain region 150 (paragraph [32]) while containing no thin gate insulating layer (see Figure 1, paragraph [08]).

Independent Claim 41. Claim 41 recites a system for electrostatic discharge protection comprising a field transistor (illustrated in Figure 2 and described in paragraphs [13] and [27]-[29]) having a source region 140 and a drain region 150 (paragraph [13] lines3-4, paragraph [28] lines 9-11) overlapped by a gate conductive layer 180 (paragraph 13 lines 10-12, paragraph [31] lines 1-5) and having a current path between the source region 140 and the drain region 150 (paragraph [32]) while containing no thin gate insulating layer (see Figure 1, paragraph [08]).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether the Examiner has substantiated that claims 1-10, 19-29, 40, and 41 are indefinite under 35 U.S.C. § 112, second paragraph, for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention.

Whether the Examiner has substantiated that claims 1-4, 7-10, 19, 23, 26, 27, and 29 are anticipated under 35 U.S.C. § 102(b) by U.S. Patent No. 5,623,154 to Murakami et al. ("Murakami et al.").

ARGUMENT

In the Final Office Action dated March 28, 2005, the Examiner rejected claims 1-10, 19-29, 40, and 41 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that Applicants regard as the invention. The Examiner also finally rejected claims 1-4, 7-10, 19, 23, 26, 27, and 29 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,623,154 to Murakami et al. ("Murakami").

Applicants respectfully ask the Board of Patent Appeals and Interferences (the "Board") to reverse the Examiner's rejection of claims 1-10, 19-29, 40, and 41 under 35 U.S.C. § 112, second paragraph, as being indefinite. Applicants respectfully request reversal of the Examiner's rejection of claims 1-4, 7-10, 19, 23, 26, 27, and 29 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,623,154 to Murakami et al. ("Murakami et al.").

The indefiniteness rejections should be reversed because the Examiner has not shown that claim term being rejected as indefinite would not reasonably apprise one of ordinary skill in the art of the scope of the claimed invention. And the anticipation rejections should be reversed because the Examiner has not substantiated that Murakami et al. teach each and every limitation in the rejected claims, as required by 35 U.S.C. § 102.

Rejection of claims 1-10, 19-29, 40, and 41 under 35 U.S.C. § 112, ¶ 2, as being indefinite

Claims 1-10, 19-29, 40 and 41 stand finally rejected under 35 U.S.C. § 112, ¶ 2 as being indefinite. All of these rejected claims contain the limitation that the claimed semiconductor device (or transistor) has a current path between a source and a drain while containing no "thin gate insulating layer." The Examiner has rejected the claims as being indefinite because the present specification does not disclose any numeric limitations about the thickness of the thin

gate oxide layer or thin gate insulating layer which would be used as a reference point in defining the difference between thick and thin. *See 3/28/05 Office Action at 3.*

Applicant respectfully disagrees that an exact numerical range needs to be described in the specification for the claim term "thin gate oxide layer" to be definite. To begin with, using a term of degree (i.e., such as thin) does not automatically render the claim indefinite. *Seattle Box Co., v. Industrial Crating & Packing, Inc.*, 731 F.2d 818, 221 USPQ 568 (Fed. Cir. 1984). When a term of degree is used, the Examiner must first determine whether the specification provides some standard for measuring that degree. But the inquiry does not conclude there. If such a standard is not present, the Examiner must inquire to whether the skilled artisan would still "reasonably" be apprised of the scope of the invention. *See M.P.E.P. § 2173.05(b).* In the final rejection, however, the Examiner has merely stopped with the first inquiry and argued that "thin" is not definite because the standard for measuring the thickness is not present in the specification, i.e., there exists no numerical range in the specification. But the Examiner has not alleged—much less argued and substantiated—that the skilled artisan would not have been reasonably apprised of the scope of "thin gate oxide layer" or "thin gate insulating layer."

Further, a definiteness inquiry under 35 U.S.C. § 112, ¶ 2 is an objective determination made in the context of whether the scope of the claim is clear to a hypothetical person possessing the ordinary level of skill in the pertinent art. The inquiry is, therefore, whether the claims set out and circumscribe a particular subject matter with a "reasonable" degree of clarity and particularity. And definiteness must be analyzed, not in a vacuum, but in light of: (i) the disclosure of the present application; (ii) the prior art; and (iii) the claim interpretation given by the skilled artisan at the time the invention was made. *See M.P.E.P. § 2173.02.* The Office, however, has primarily focused only on factor (i).

Turning to factor (i), the present specification describes and illustrates in several instances a thin gate insulating layer, describes their functions, and describes the differences between devices containing a thin gate insulating layer and the claimed inventive devices not having a thin gate insulating layer. *See Paragraphs [07], [08], & [032-033].* While it is true that the specification does not give an exact thickness (or range of thicknesses) for the thin gate insulating layer, such information reasonably apprises the skilled artisan of what is a thin gate insulating layer. For this reason alone, the rejection is improper.

Turning to factor (ii), the prior art, Applicants submitted search results showing that at least 42 patents since 1976 have issued with "semiconductor" and "thin gate oxide layer" phrases in the claims. The Examiner considered such evidence to be non-persuasive and contended that merely citing 42 results of a search engines does not reflect what each of the 42 underlying disclosures teach about this claim term. The Examiner cited to Nishida et al. (U.S. Patent No. 3789503) and Hsu et al. (U.S. Patent No. 6841821) as showing a difference of 1600 Angstroms between what each reference describes as a thin gate oxide layer. The Examiner concluded that it would be improper to assume a definite meaning for this term where multiple definitions are taught by the prior art.

The Examiner's reliance on these two patents is not legally or factually sufficient to support the argument of the existence of a wide disparity of thicknesses for a thin gate oxide layer. The time frame for inquiring about indefiniteness is—as noted above—at the time of the invention. In the present application, the "time of the invention" of the present application is currently based on the effective filing date of the application, or early 2001. Nishida et al. (1974), however, is much earlier than this time frame by 27 years and Hsu et al. (2005) is later than this time frame by several years.

More importantly, as any skilled artisan can testify, the size and dimensions of semiconductor devices have been decreasing for many years.[3] Thus, the gate oxide thickness disclosed by Nishida et al. (in 1974) would necessarily be different (i.e., larger) than the gate oxide thickness disclosed by Hsu et al. (in 2005). Indeed, the skilled artisan would have expected such a wide difference because of the trends in semiconductor technology. Thus, the disclosures of 2 patents more than 30 years apart does not adequately show the teachings of the prior art (which must be considered when analyzing definiteness).

Perhaps the most pertinent evidence submitted by Applicants is U.S. Patent No. 6,586,306 ("the '306 Patent"; attached in the Evidence Appendix as Evidence Appendix D at page 36). The '306 Patent has an effective filing date at nearly the same time as the present application. The '306 Patent contains a claim (claim 1) for making a semiconductor device, including the steps of forming a "thin gate oxide layer" in one region and a "thick gate oxide layer" in another region. Importantly, despite the existence of these two claim terms, there exists no numerical range for "thin" or "thick" in the specification of the '306 Patent, at least none that the undersigned could locate. Yet the '306 Patent was allowed with both of these terms in the claims.

Thus, the Office itself has previously issued claims with a nearly identical term as recited in the present claims, yet where there also existed no numerical range in the specification. How can an application with "thin gate oxide layer" and no numerical range in the specification be issued as the '306 Patent (and therefore, by definition, be valid and definite) on the one hand, yet on the other hand be deemed not definite in the present application? It seems both an illogical and an untenable position.

---

[3] Indeed, this knowledge is recognized even outside the semiconductor art.

Further, a cursory review of the previously cited 42 patents showed that the '306 Patent was not an aberration. The Office also issued U.S. Patent No. 6,124,172 (the "'172 Patent" attached in the Evidence Appendix as Evidence Appendix E at page 47) that contained the term "thin gate oxide layer" in the claims (claim 24), but without a numerical range for the thickness present in the specification. In fact, the '172 Patent never uses the phrase "thin gate oxide layer" anywhere else in the specification, or even the single term "thin." It is no doubt likely that Applicants could presumably find additional examples in the prior art, e.g., by additional analysis and/or by changing the search parameters. But two patents are sufficient to illustrate that the claims set out and circumscribe a particular subject matter with a reasonable degree of clarity and particularity in light of the prior art.

Turning to factor (iii) of M.P.E.P. § 2173.02, a skilled artisan would have understood that "thin" gate oxide layer sets out and circumscribes a particular subject matter with a "reasonable" degree of clarity and particularity. Applicants previously filed a Declaration under 37 C.F.R. § 1.132 (the "Declaration") evidencing that the skilled artisan would have understood that a "thin gate oxide layer" or "thin gate insulating layer" is reasonably clear and precise. *See Declaration in the Evidence Appendix as Evidence Appendix C at page 33.* The Declaration was signed by Taeg-Hyun Kang, one of the inventors, and originally submitted with the Request for Reconsideration submitted on June 28, 2005.

The Declaration, however, was erroneously not entered or considered by the Examiner. In the Advisory Action dated August 9, 2005, the Examiner indicated that he did not enter the Declaration because it was filed after the date of filing a Notice of Appeal and failed to overcome all rejections and/or was filed without a showing of good and sufficient reasons why it was necessary and was not earlier presented. At that time the Declaration was filed, Applicants

had not yet filed a Notice of Appeal. The correct standard for admission, therefore, should have been a showing of good and sufficient reasons why the Declaration is necessary and was not earlier submitted. *37 C.F.R. § 1.116.*

Applicants, however, previously provided these good and sufficient reasons in the Request for Reconsideration that was submitted with the Declaration. The rejection by the Examiner under 35 U.S.C. § 112, second paragraph, of the indefiniteness of the "thin gate insulating layer" was only provided in the Office Action dated August 19, 2004. In response, Applicants submitted voluminous evidence that the term was well understood in the art, believing that a submission under 37 C.F.R. § 1.132 was not necessary. The Examiner then refused Applicants' arguments and made the rejection final on March 28, 2005. The Declaration was then submitted at the next possible time, with the Request for Reconsideration, along with the requisite showing (see Request for Reconsideration at pages 5-6, and the text of the Declaration itself).

The Declaration therefore should have been entered, as required by both M.P.E.P. § 714.12 and 37 C.F.R. § 1.116.

> An affidavit or other evidence filed after a final rejection, but before or on the same date of filing an appeal, may be entered upon a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented.

M.P.E.P. § 714.12 (emphasis added). Applicants therefore request that the Declaration be entered and considered on Appeal.

Considering all of the evidence, it is clear that the Examiner has not met the requisite burden of showing that "thin gate oxide layer" would render the claims indefinite to the skilled artisan. Accordingly, Applicants respectfully request that the Board reverse the Examiner's rejections under 35 U.S.C. § 112, ¶ 2.

Rejection of claims 1-4, 7-10, 19, 23, 26, 27, and 29 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,623,154 to Murakami

Claims 1-4, 7-10, 19, 23, 26, 27, and 29 under 35 U.S.C. § 102(b) stand rejected as being anticipated by Murakami et al. (U.S. Patent No. 5,623,154). The Office argues that Murakami et al. teach the claimed invention in the device depicted in Figure 1 of this prior art reference.

M.P.E.P. § 2131 sets forth the standard for a rejection of a claim as anticipated under 35 U.S.C. § 102. "To anticipate a claim, the reference must teach every element of the claim." M.P.E.P. § 2131 further states that

> "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). . . . "The identical invention must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants respectfully submit that the Examiner has not shown that Murakami et al. teaches every element of the rejected claims and so has not substantiated that the claims are anticipated by Murakami et al.

As is evident from the Claims Appendix, all independent claims contain the limitation that the transistor has a current path between a source and a drain while containing no thin gate insulating layer. As described in paragraphs [11] and [32]-[33] of the present specification, the transistor described contains an inversion layer (135) that provides a current path between the source and drain regions, yet without using a thin gate insulating layer, thereby protecting against ESD stress. The prior art devices (as illustrated in Figure 1) were unable to protect against the ESD stress because the thin gate insulating layer (19) in the transistor would break down. *See also paragraphs [07] and [08].*

The Examiner has not substantiated that Murakami et al. discloses this limitation in the rejected independent claims. This reference discloses an NMOS transistor 20 containing source and drain regions 11, a gate oxide film 15, and a gate electrode layer 17. *See column 7, lines 26-50 and Figure 1.* As recognized by the skilled artisan and as supported in the remainder of Murakami et al., the gate oxide film 15 would operate as a thin gate insulating layer of the NMOS transistor. Indeed, Murakami et al. discloses that the insulating layer is a thin gate oxide layer. *Column 2 lines 30-32.* Indeed, based on the structure of the NMOS transistor 20 depicted in Figure 1 of Murakami et al., it would be difficult—if not impossible—for the Examiner to substantiate that NMOS transistor 20 contains no thin gate insulating layer.

The Examiner argues that Murakami et al. describe a field transistor with the claimed features and containing "no gate insulating layer." But this is not what the claims recite. The rejected claims recite "no thin gate insulating layer." It appears that the Examiner has ignored the presence of the term "thin," because of the improper indefiniteness rejection.

But the Examiner cannot eliminate this term from the claim when rejecting the claims over Murakami et al. All words in a claim must be considered in judging the patentability of a claim against the prior art. *In re Wilson*, 424 F.2d 1382, 165 USPQ 494 (CCPA 1970). Where the degree of uncertainty about the definiteness of a claim term is not great, the Examiner should reject the claims based on indefiniteness and based on prior art, but "based on the interpretation of the claims which renders the prior art applicable." *See M.P.E.P. § 2173.06; cf Ex parte Ionescu*, 222 USPQ 537 (Bd. App. 1984). When making a rejection over prior art in these circumstances, it is important for the Examiner to point out how the claim is being interpreted. *See M.P.E.P. § 2173.06.* But nowhere is the Examiner allowed to just ignore the claim term altogether.

The Examiner, however, has failed to adhere to these standards. Accordingly, the Examiner has not substantiated that Murakami et al. teaches each and every limitation in the rejected claims. Applicants note—for the record—that they requested repetition of the final rejection in accordance with M.P.E.P. § 2173.06. *See 7/28/05 Request for Reconsideration at 7.* The Examiner did not honor this request.

Accordingly, Applicants respectfully request the Board to reverse the rejection under 35 U.S.C. § 102(b) of claims 1-4, 7-10, 19, 23, 26, 27, and 29 as being anticipated by Murakami et al.

Conclusion

For the reasons set forth above, as well as those previously of record, Applicants respectfully request the Board to reverse the Examiner's rejections of the pending claims.

If there is any fee due in connection with the filing of this Appeal Brief, including a fee for any extension of time not previously accounted for, please charge the fee to our Deposit Account No. 50-0843.

Respectfully submitted,

Kenneth E. Horton
Registration No. 39,481

KIRTON & McCONKIE
1800 Eagle Gate Tower
60 East South Temple
Salt Lake City, Utah 84111
Telephone: (801) 328-3600
Facsimile: (801) 321-4893

CLAIMS APPENDIX

1. A field transistor having a current path between a source and a drain while containing no thin gate insulating layer, the transistor comprising:

a well region of a first conductivity type;

a field oxide layer for defining an active region on the well region;

high concentration source and drain regions of a second conductivity type separated from each other by a width of the field oxide layer;

a low concentration source region of the second conductivity type formed in the well region, the low concentration source region being adjacent to the high concentration source region and overlapped by one end of the field oxide layer;

a low concentration drain region of the second conductivity type formed in the well region, the low concentration drain region being adjacent to the high concentration drain region and overlapped by the other end of the field oxide layer; and

a gate conductive layer pattern formed on the field oxide layer, the gate conductive layer pattern overlapping parts of the low concentration source and drain regions of the second conductivity type.

2. The field transistor of claim 1, wherein the well region of the first conductivity type is formed on a high concentration buried region of the first conductivity type on a semiconductor substrate of the first conductivity type.

3. The field transistor of claim 1, wherein the well region of the first conductivity type is formed on a semiconductor substrate of the first conductivity type.

4. The field transistor of claim 1, further comprising a high concentration diffusion region of the first conductivity type formed in the well region, the high concentration diffusion

region being separated from the high concentration source region of the second conductive type by a predetermined distance.

5. The field transistor of claim 4, further comprising a low concentration diffusion region of the first conductivity type and a low concentration diffusion region of the second conductivity type, both low concentration diffusion regions being adjacent to each other between the high concentration diffusion region of the first conductivity type and the high concentration source region of the second conductivity type.

6. The field transistor of claim 5, wherein the low concentration diffusion region of the first conductivity type is adjacent to the high concentration diffusion region of the first conductivity type, and the low concentration diffusion region of the second conductivity type is adjacent to the high concentration source region of the second conductivity type.

7. The field transistor of claim 1, further comprising:

a gate electrode electrically connected to the gate conductive layer pattern;

a source electrode electrically connected to the high concentration source region of the second conductivity type; and

a drain electrode electrically connected to the high concentration drain region of the second conductivity type.

8. The field transistor of claim 7, wherein the drain electrode is electrically connected to the gate electrode.

9. The field transistor of claim 7, wherein the source electrode is electrically connected to the high concentration diffusion region of the first conductivity type as well.

10. The field transistor of claim 1, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

11. (withdrawn)

12. (withdrawn)

13. (withdrawn)

14. (withdrawn)

15. (withdrawn)

16. (withdrawn)

17. (withdrawn)

18. (withdrawn)

19. A semiconductor device having a current path between a source and a drain while containing no thin gate insulating layer, the transistor comprising:

a substrate comprising a well region of a first conductivity type;

a field oxide layer located over a portion of the well region;

a first source region of a second conductivity type and a first drain region of a second conductivity type separated by the field oxide layer;

a second source region having a second conductivity type concentration lower than the first source region, the second source region formed in the well region adjacent the first source region with a portion of the second source region underlying the field oxide layer;

a second drain region having a second conductivity type concentration lower than the first drain region, the second drain region formed in the well region adjacent the first drain region with a portion of the second drain region underlying the field oxide layer; and

a conductive layer formed over the field oxide layer, the conductive layer overlapping the second source region and the second drain region.

20. The device of claim 19, further comprising a first diffusion region of the first conductivity type formed in the well region and separated from the first source region.

21. The device of claim 20, further comprising a second diffusion region having a first conductivity type concentration lower than the first diffusion region and comprising a third diffusion region of the second conductivity type, both the second and third diffusion regions adjacent each other and located between the first diffusion region and the first source region.

22. The device of claim 21, the second diffusion region type located adjacent the first diffusion region and the third diffusion region located adjacent the first source region.

23. The device of claim 19, further comprising:

a gate electrode electrically connected to the conductive layer;

a source electrode electrically connected to the first source region; and

a drain electrode electrically connected to the first drain region.

24. The device of claim 23, the drain electrode being electrically connected to the gate electrode.

25. The device of claim 23, the source electrode being electrically connected to the first diffusion region.

26. The device of claim 19, wherein the first conductivity type is p-type and the second conductivity type is n-type.

27. A semiconductor device having a current path between a source and a drain while containing no thin gate insulating layer, the transistor comprising:

a substrate comprising a well region of a first conductivity type;

a field oxide layer located over the well region;

a first source region of a second conductivity type and a first drain region of a second conductivity type separated by the field oxide layer;

a second source region having a second conductivity type concentration lower than the first source region, the second source region formed in the well region adjacent the first source region with a portion of the second source region underlying the field oxide layer;

a second drain region having a second conductivity type concentration lower than the first drain region, the second drain region formed in the well region adjacent the first drain region with a portion of the second drain region underlying the field oxide layer;

a conductive layer formed over the field oxide layer, the conductive layer overlapping the second source region and the second drain region;

a gate electrode electrically connected to the conductive layer;

a source electrode electrically connected to the first source region; and

a drain electrode electrically connected to the first drain region.

28. The device of claim 27, further comprising a first diffusion region of the first conductivity type formed in the well region and separated from the first source region, a second diffusion region having a first conductivity type concentration lower than the first diffusion region, and a third diffusion region of the second conductivity type, wherein both the second and third diffusion regions are adjacent each other and located between the first diffusion region and the first source region.

29. A system for electrostatic discharge protection containing a field transistor having a current path between a source and a drain without a thin gate insulating layer, the field transistor comprising:

a substrate comprising a well region of a first conductivity type;

a field oxide layer located over the well region;

a first source region of a second conductivity type and a first drain region of a second conductivity type separated by the field oxide layer;

a second source region having a second conductivity type concentration lower than the first source region, the second source region formed in the well region adjacent the first source region with a portion of the second source region underlying the field oxide layer;

a second drain region having a second conductivity type concentration lower than the first drain region, the second drain region formed in the well region adjacent the first drain region with a portion of the second drain region underlying the field oxide layer; and

a conductive layer formed over the field oxide layer, the conductive layer overlapping the second source region and the second drain region.

30. (withdrawn)

31. (withdrawn)

32. (withdrawn)

33. (withdrawn)

34. (withdrawn)

35. (withdrawn)

36. (withdrawn)

37. (withdrawn)

38. (withdrawn)

39. (withdrawn)

40. A semiconductor device for electrostatic discharge protection, the device comprising a field transistor having both a source region and a drain region overlapped by a gate

conductive layer and having a current path between the source region and the drain region while containing no thin gate insulating layer.

41. A system for electrostatic discharge protection, the system comprising a field transistor having both a source region and a drain region overlapped by a gate conductive layer and having a current path between the source region and the drain region while containing no thin gate insulating layer.

EVIDENCE APPENDIX

FIG. 1 (PRIOR ART)

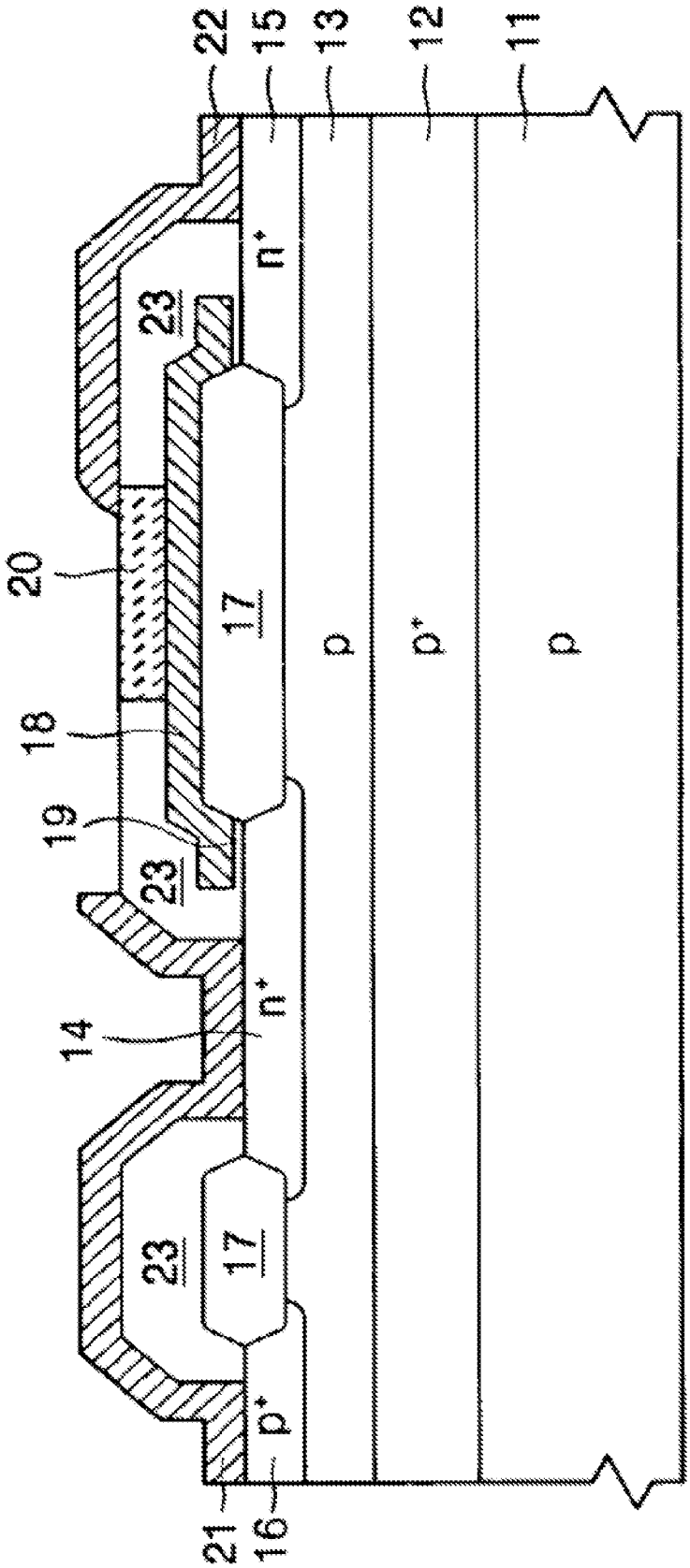
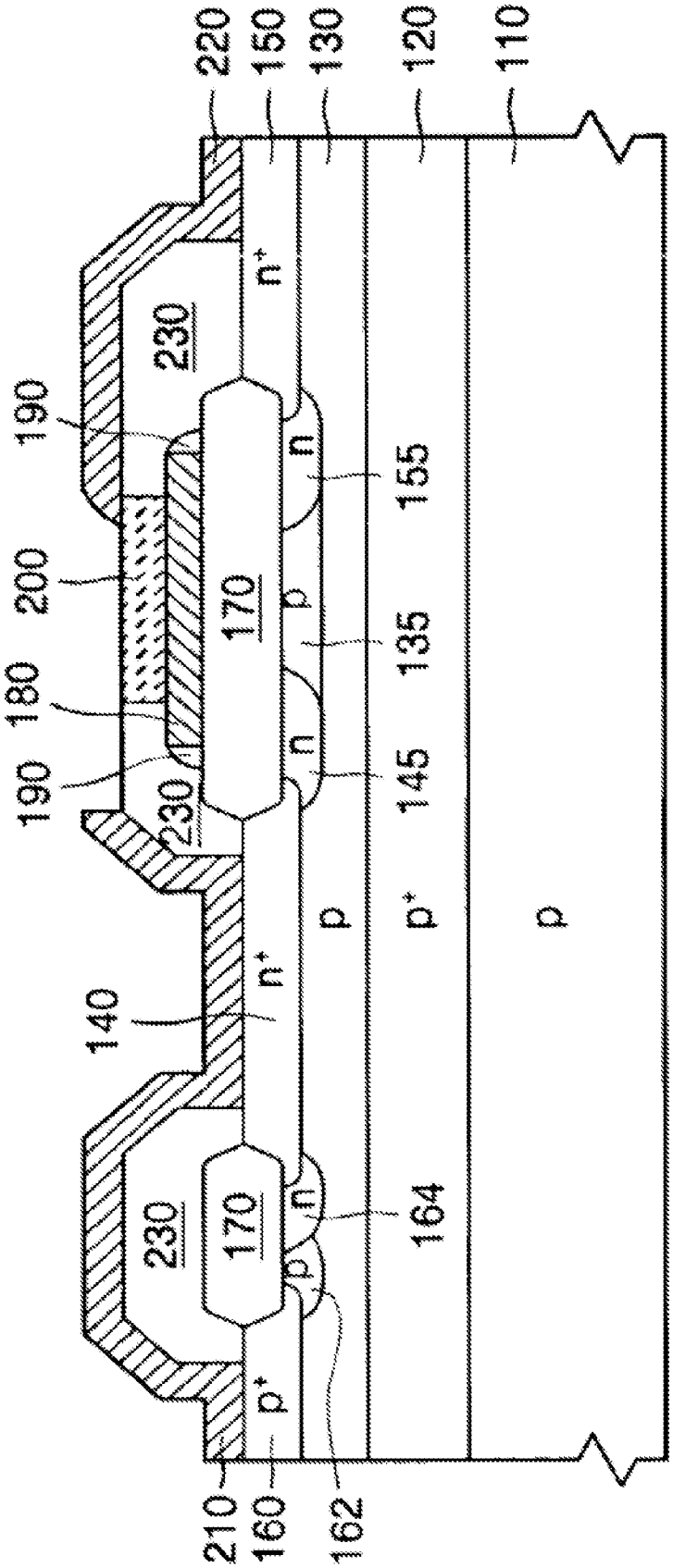


FIG. 2


220
150
130
120
110
230
190
n+
n
155
200
170
p
135
180
190
n
145
230
p
p+
p
140
n+
230
170
n
164
p
p+
210
160
162

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application:
Taeg-Hyun Kang, et al.

Serial No.: 10/071,494

Filed: February 6, 2002

For: FIELD TRANSISTORS FOR ELECTROSTATIC DISCHARGE PROTECTION AND METHODS FOR FABRICATING THE SAME

Confirmation No. 1924

Group Art Unit: 2826

Examiner: V. Mandala

Mail Stop After-Final Response
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

DECLARATION UNDER 37 C.F.R. § 1.132

I, the undersigned, declare that:

1. I am one of the inventors of the subject matter in the above-captioned patent application;

2. I have been informed that the claims have not been allowed because the Examiner considers the phrase "thin gate insulating layer" to not be definite because there exists no numerical range of the thickness of the layer in the specification.

3. I consider myself to be "one with ordinary skill in the art" in the semiconductor industry. I base this consideration on my qualifications, which include a B.S. in Applied

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450, on this 28th Day of June, 2005.

Signed: Erin Fowler

Engineering from the Samsung Institute of Management and Technology. I majored in electrical engineering at the University of Incheon as a part time student and acquired a wide knowledge of integrated circuit design, methodology, and fabrication, as well as programming languages, ESD cell device optimization, and RF simulation. I have also acquired a wide knowledge in the integrated chip design industry through more than 14 years of maintaining and supporting TCAD software.

4. In a transistor of a semiconductor device, the gate insulating layer (usually silicon dioxide and therefore a gate oxide layer) lies between the gate electrode, which turns the current flow on and off, and the channel through which this current flows. The gate oxide layer, in essence, acts as an insulator, protecting the channel from the gate electrode and preventing a short circuit.

5. By reducing the thickness of the gate oxide layer, it is possible to increase the transistor's switching speed. That result is due to the electrode being even closer to the channel, thereby inducing a larger current to flow through the transistor. However, thinner oxide layers degrade at lower voltages, and their behavior is more difficult to understand than the behavior of thicker oxides. As a result, the dimensions of a gate oxide layer are thin enough to assure the performance of the transistor and not under such a high electric field to induce its degradatation, whether a field oxide is thick enough to isolate transistors.

6. A thin gate oxide is formed on an active region that is defined by the field oxide in the substrate. Accordingly, a field transistor with no thin gate oxide can be understood as a field transistor of which the gate electrode does not extend onto the active region. Therefore, the thin gate oxide (considered to be formed on the active region) is distinguished from the field oxide.

7. That all statements are made of my own knowledge are true and all statements made on information and belief are believed to be true; and, further, that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code, and that such willful, false statements may jeopardize the validity of the application or any patent issuing thereon.

TaegHyun KANG 06/22/05

Name Date

US006586306B2

(12) **United States Patent**
Lee et al.

(10) **Patent No.: US 6,586,306 B2**
(45) **Date of Patent: Jul. 1, 2003**

(54) **METHOD FOR FABRICATING SEMICONDUCTOR DEVICE**

(75) Inventors: **Hi Deok Lee**, Chungcheongbuk-do (KR); **Seong Hyung Park**, Chungcheongbuk-do (KR)

(73) Assignee: **Hynix Semiconductor Inc.**, Kyoungki-do (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/125,271**

(22) Filed: **Apr. 18, 2002**

(65) **Prior Publication Data**

US 2002/0153562 A1 Oct. 24, 2002

(30) **Foreign Application Priority Data**

Apr. 24, 2001 (KR) 2001-0021936

(51) **Int. Cl.**[7] **H01L 21/336**; H01L 21/335; H01L 21/8232

(52) **U.S. Cl.** **438/305**; 438/303; 438/142

(58) **Field of Search** 438/142, 303, 438/305, 423, 520, 528

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,200,834 B1 * 3/2001 Bronner et al. 438/303
6,271,572 B1 * 8/2001 Fujita 257/392
6,410,391 B1 * 6/2002 Kawai et al. 438/423
6,495,896 B1 * 12/2002 Yagashi et al. 257/500

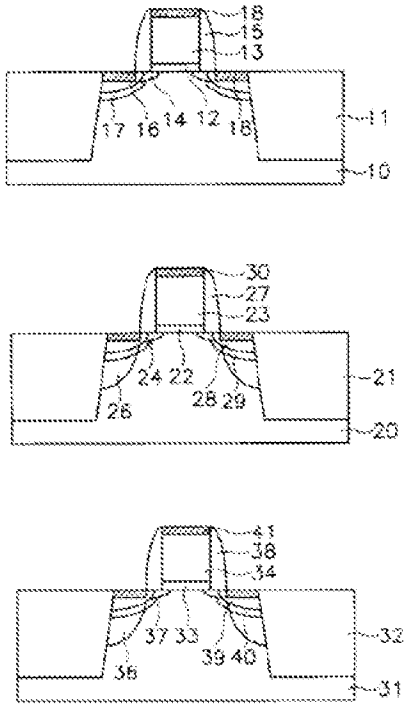
* cited by examiner

Primary Examiner—John F. Niebling
Assistant Examiner—Walter L. Lindsay, Jr.
(74) *Attorney, Agent, or Firm*—Marshall, Gerstein & Borun

(57) **ABSTRACT**

A method for fabricating a semiconductor device is disclosed. In a high speed device structure consisting of a salicide, in order to fabricate a device having at least two gate oxide structures in the identical chip, an LDD region of a core device region is formed, and an ion implant process for forming the LDD region of an input/output device region having a thick gate oxide and a process for forming a source/drain region at the rim of a field oxide of the core device region having a thin gate oxide are performed at the same time, thereby increasing a depth of a junction region. Thus, the junction leakage current is decreased in the junction region of the peripheral circuit region, and the process is simplified. As a result, a process yield and reliability of the device are improved.

15 Claims, 6 Drawing Sheets



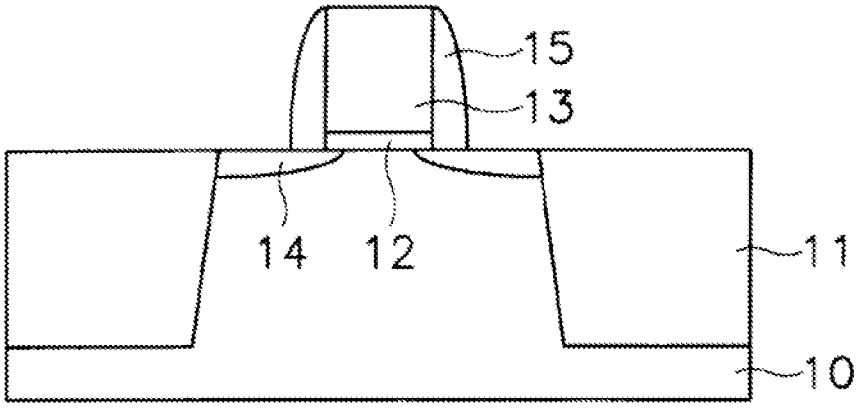


Fig.1A

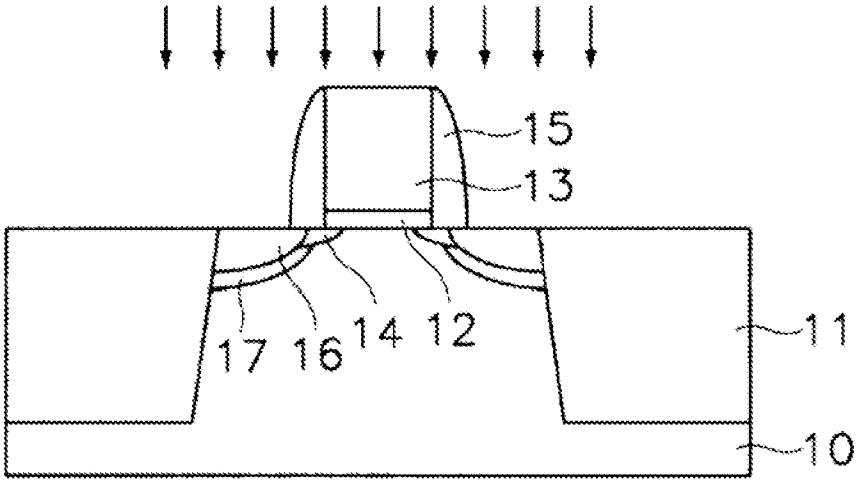


Fig.1B

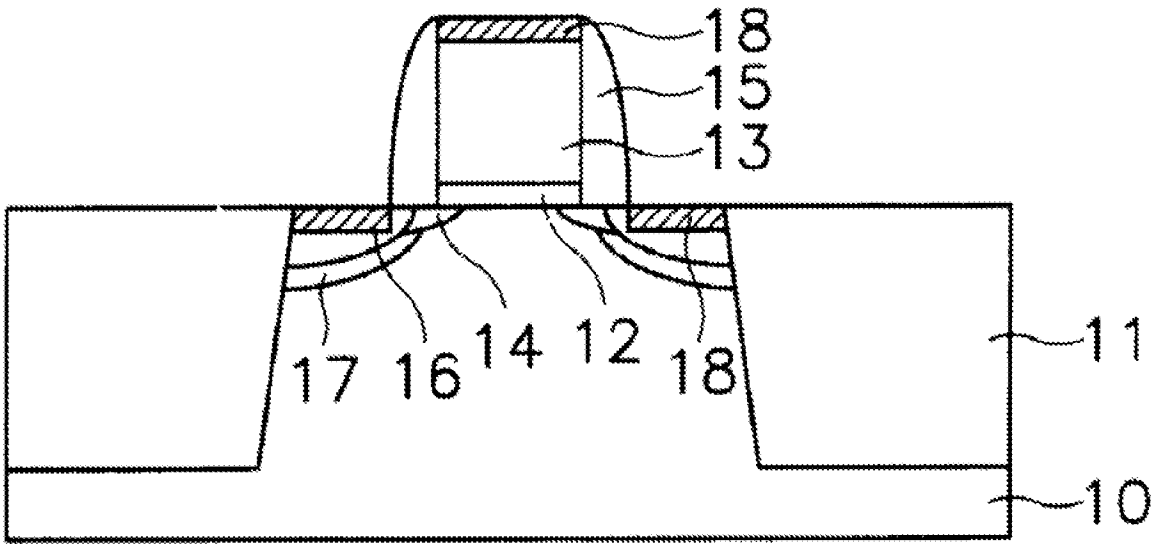


Fig.1C

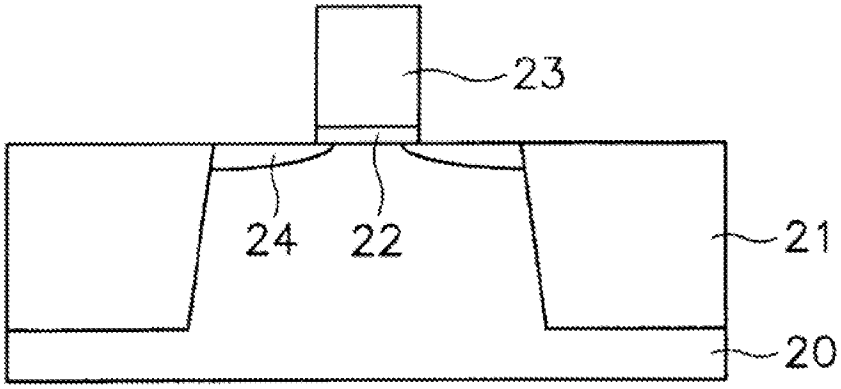


Fig.2A

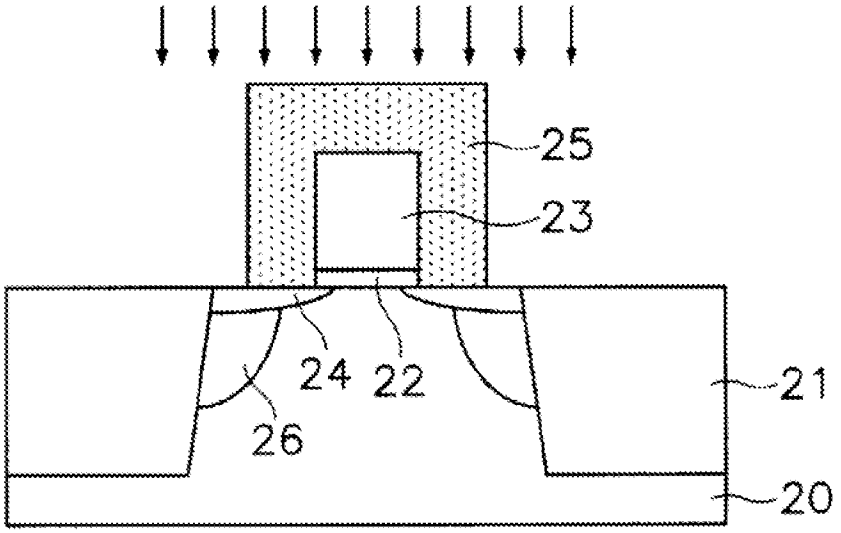


Fig.2B

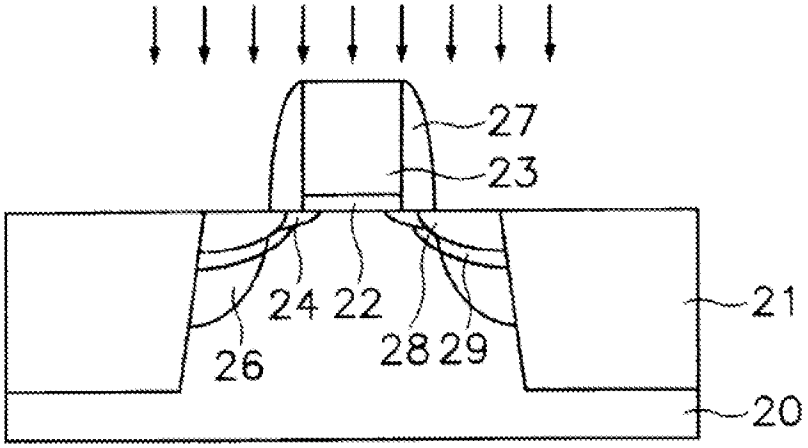


Fig.2C

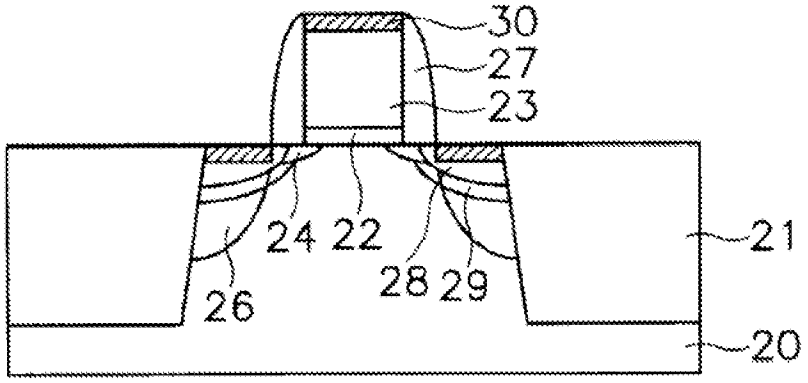


Fig.2D

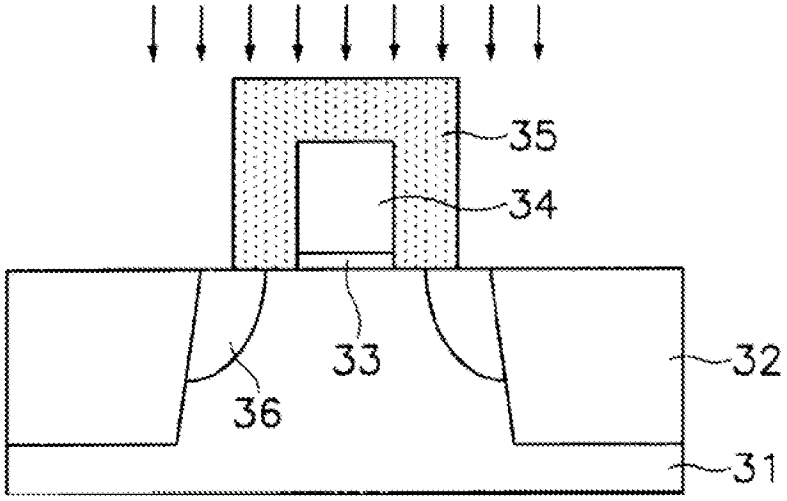


Fig.3A

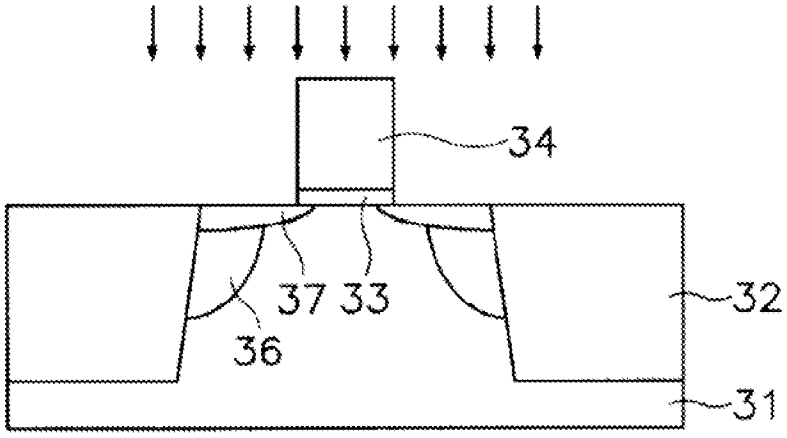


Fig.3B

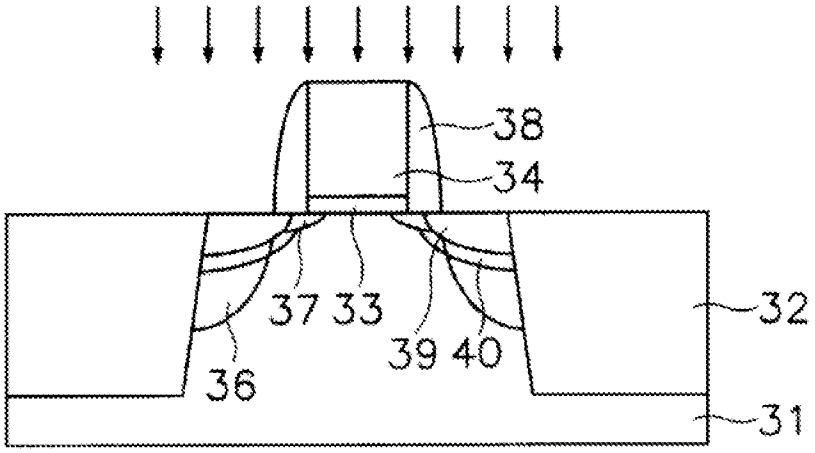


Fig.3C

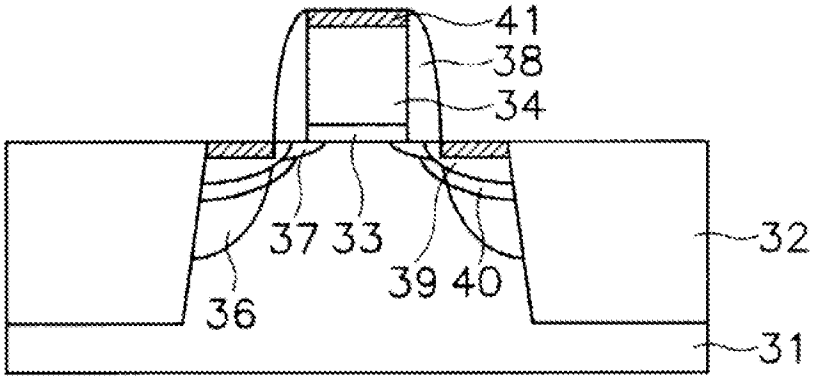


Fig.3D

METHOD FOR FABRICATING SEMICONDUCTOR DEVICE

BACKGROUND

1. Technical Field

A method for fabricating a semiconductor device is disclosed. In particular, an improved method for fabricating a semiconductor device is disclosed which provides a difference in junction depth by performing at least one implant process for forming an LDD region in a MOSFET having a thin gate oxide in a high speed device having a salicide (self-aligned silicide).

2. Description of the Related Art

In general, the most important function of a transistor of a semiconductor circuit is a current driving function. A channel width of a metal-oxide-semiconductor field effect transistor (MOSFET) is adjusted in consideration of the current driving function. In the most widely-used MOSFET, an impurity-doped polysilicon layer is used as a gate electrode, and a diffusion region formed by doping an impurity on a semiconductor substrate is used as a source/drain region.

A buried channel is formed in a positive metal-oxide-semiconductor field effect transistor (PMOSFET) which uses an N+ doped polysilicon gate electrode in a complementary metal-oxide-semiconductor field effect transistor (CMOSFET). Here, because a negative metal-oxide-semiconductor field effect transistor (NMOSFET) with a channel on its surface and the PMOSFET have different threshold voltages, there are various restrictions in design and fabrication of the device.

That is, in the CMOSFET using a dual gate electrode, the dual gate electrodes are formed by ion-implanting N-type and P-type impurities twice. Therefore, a photolithography process should be performed twice, and this complicates the fabrication process. Accordingly, the device is easily contaminated due to a wet process, and thus the process yield and reliability of the devices are reduced.

FIGS. 1A through 1C are cross-sectional views illustrating sequential steps of a conventional method for fabricating such a semiconductor device which is an example of a MOSFeT having a thin gate oxide film.

First, referring to FIG. 1A, a field oxide **11** defining an active region is formed on a semiconductor substrate **10**. A thin gate oxide **12** and a polysilicon layer (not shown) are formed on the semiconductor substrate **10**. Thereafter, the polysilicon layer is etched using a gate electrode mask as an etching mask, to form a gate electrode **13**. An LDD (lightly doped drain) region **14** is formed by ion-implanting a low concentration impurity to the semiconductor substrate **10** at both sides of or around the gate electrode **13**. An insulating film spacer **15** is formed at side walls of the gate electrode **13**.

As shown in FIG. 1B, a first source/drain region **16** is formed by ion-implanting a high concentration impurity to the semiconductor substrate **10** at both sides of or around the insulating film spacer **15**. Thereafter, a second source/drain region **17** is formed by implanting a dopant having a high diffusion ratio at a low dose.

As shown in FIG. 1C, a silicide layer **18** is then formed on the surfaces of the gate electrode **13**, and the semiconductor substrate.

However, the conventional method for fabricating the semiconductor device has a limit due to a shallow junction region resulting from miniaturization of the device. Specifically, the depth of the junction region is increased by the ion implant process for forming the silicide layer **18**, which influences the LDD region **14** due to the close proximity of the silicide layer **18** to the LDD region **14** as shown in FIG. 1C. Further, when the silicide layer **18** is formed deeply along the rim of the field oxide, a leakage current is considerably increased in the junction region adjacent to the field oxide **11**. Still further, as the height of the field oxide is decreased during subsequent processes, the leakage current increases.

SUMMARY OF THE INVENTION

Accordingly, a method for fabricating a semiconductor device is disclosed which can prevent an increase of the junction leakage current and which can improve the process yield and reliability, by forming a deep junction near the field oxide which does not influence the channel region of a MOSFET where a gate oxide is thin (hereinafter referred to as "a core device"), by partially exposing a source/drain region adjacent to the field oxide to a photolithography process for forming an LDD region of an input/output device between the core device and a MOSFET where the gate oxide film (hereinafter referred to as "a input/output device) is thick in a CMOS fabrication process, and by ion-implanting an impurity thereto at the same time an ion implant process is carried out for forming the LDD region of the input/output device region.

A disclosed method for fabricating a semiconductor device comprises: forming a field oxide defining an active region on a semiconductor substrate having a central core device region and a peripheral input/output device region; forming a gate oxide on the core device region; forming a gate electrode on the gate oxide; forming a first LDD region by ion-implanting a low concentration of impurity ions to the input/output device region of the active region; forming a photoresist film pattern over the gate electrode and on the sides of the gate electrode, the photoresist film pattern reaching from an end of the gate oxide to a part of input/output device region spaced a determined distance from the gate electrode or gate oxide; forming a second LDD region deeper than the first LDD region by implanting a low concentration of impurity ions by using the photoresist film pattern as an ion implant mask; removing the photoresist film pattern; forming an insulating film spacer on side walls of the gate electrode; forming a deep source/drain region and a shallow source/drain region by implanting a high concentration impurity ions to the input/output device region of the active region of the semiconductor substrate at least once, by using the insulating film spacer as an ion implant mask; and forming a silicide film on the gate electrode and the source/drain regions.

A novel semiconductor device made in accordance with the methods disclosed herein is also disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

The disclosed methods and devices will become better understood with reference to the accompanying drawings which are given only by way of illustration and thus are not limitative of the disclosure, wherein:

FIGS. 1A through 1C are cross-sectional views illustrating sequential steps of a conventional method for fabricating a semiconductor device;

FIGS. 2A through 2D are cross-sectional views illustrating sequential steps of a method for fabricating a semiconductor device in accordance with a first embodiment; and

FIGS. 3A through 3D are cross-sectional views illustrating sequential steps of a method for fabricating a semiconductor device in accordance with a second embodiment.

DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS

A method for fabricating a semiconductor device in accordance with preferred embodiments will now be described in detail with reference to the accompanying drawings.

FIGS. 2A through 2D are cross-sectional views illustrating sequential steps of a method for fabricating a semiconductor device in accordance with a first embodiment. A core device region is shown in an NMOS region or PMOS region of a CMOS.

First, referring to FIG. 2A, a field oxide **21** defining an active region is formed on a semiconductor substrate **20**. The active region defined by the field oxide can be further characterized as including a central core device region and a peripheral input/output device region. A gate oxide **22** is formed on the active region of the semiconductor substrate **20**. A polysilicon layer (not shown) is formed on the gate oxide **22**. Here, the gate oxides **22** in the core device region and the input/output device region are formed to be different thickness.

Thereafter, the polysilicon layer is etched using a gate electrode mask as an etching mask, to form a gate electrode **23** on the gate oxide **22** in the core device region and the input/output device region, respectively. A first LDD region **24** is formed by ion-implanting a low concentration impurity ions to the semiconductor substrate **20** at both sides of or around the gate electrode **23** in the core device region. At this time, the ion implant process is performed at a dose ranging from about 1×10^{13} to about 2×10^{14} ions/cm^2 with an ion implant energy ranging from about 10 to about 50 keV.

When the core device region is a PMOS region, the ion implant process is performed using BF_2, B_{11}, or In as a dopant. In the case that core device region is a NMOS region, the ion implant process is performed using As or P as the dopant.

Referring to FIG. 2B, a photoresist film pattern **25** is formed to partially expose the first LDD region **24** at the inner rim of the field oxide **21** in the core device region. The photoresist pattern **25** is used as an LDD ion implant mask in the input/output device region.

Then, an impurity is ion-implanted to the exposed portion of the input/output device region and the first LDD region **24** by using the photoresist film pattern **25** as an ion implant mask, thus forming a second LDD region **26**. Here, the ion implant process is performed at a dose ranging from about 1×10^{13} to about 2×10^{15} ions/cm^2 with an ion implant energy ranging from about 10 to about 50 keV. The second LDD region **26** has a deeper profile than the first LDD region **24** (see FIG. 2B).

Referring to FIG. 2C, the photoresist film pattern **25** is then removed and an insulating film spacer **27** is formed at sides walls of the gate electrode **23**. A first source/drain region **28** is formed by ion-implanting a high concentration impurity to the semiconductor substrate **20** **25** at both sides of or around the insulating film spacer **27**.

Still referring to FIG. 2C, a second source/drain region **29** is formed by ion-implanting a high concentration impurity to the semiconductor substrate **20** at both sides of or around the insulating film spacer **27**. Here, the ion implant processes for forming the first source/drain region **28** and the second source/drain region **29** are performed at a dose ranging from about 1×10^{15} to about 1×10^{16} ions/cm^2 with an ion implant energy ranging from about 5 to about 60 keV. In the case of the PMOS, the ion implant process is carried out by using BF_2, B_{11}, or In. In the case of the NMOS, the ion implant process is performed by using As or P. In addition, heavy ions are used among the identical conductive type doses when forming a shallow region such as the first source/drain region **28**, and light ions are used when forming a deep region such as the second source/drain region **29**.

As shown in FIG. 2D, a silicide layer **30** is formed on the gate electrode **23** and the first and second source/drain regions **28**, **29**.

FIGS. 3A through 3D are cross-sectional diagrams illustrating sequential steps of a method for fabricating a semiconductor device in accordance with a second embodiment. As compared with the first embodiment, the processes of FIGS. 2A and 2B are performed in a different order.

Turning first to FIG. 3A, a substrate **31** is provided with a field oxide **32** that defines an active region that can be characterized as including a central core region and a peripheral input/output device region. A gate oxide **33** and gate electrode **34** are disposed in the active region. A photoresist film pattern **35** is then formed to partially expose the core device region at the inner rim of the field oxide. Then, an impurity is ion-implanted to the exposed portion of the core device region of the substrate **31** using the photoresist film pattern **35** as an ion implant mask, thus forming a first LDD region **36**.

Turning to FIG. 3B, the photoresist film pattern **35** is removed and a second ion implantation step is carried out at a low concentration of impurity ions to form a second LDD region **37**.

Turning to FIG. 3C, an insulation film spacer **38** is then formed on the sidewall or sidewalls of the gate electrode **34**/gate oxide **33** structure. Then, a first source/drain region **39** is formed by ion-implanting a high concentration of impurity ions to the semiconductor substrate **31** around the insulating film spacer **38**. Subsequently, a second source/drain region **40** is formed by ion/implanting another high concentration of impurity ions to the semiconductor substrate **31** around the insulating film spacer **27**. The first source/drain region **39** is formed using heavy ions while the second source/drain region **40** is formed using lighter ions. Then, as shown in FIG. 3D, a silicide layer **41** is formed on top of the gate electrode **34** and the first and second source/drain regions **39**, **40**.

As described earlier, in the high speed device structure consisting of a self-aligned salicide, in order to fabricate a device having at least two gate oxide structures in the identical chip, the LDD region of the core device is formed, and the ion implant process for forming the LDD region of the input/output device having a thick gate oxide and the process for forming the source/drain region at the rim of the field oxide of the core device having a thin oxide film are performed at the same time, thereby increasing the depth of the junction region. Thus, a junction leakage current is decreased in the junction region of the peripheral circuit region, and the whole process is simplified without requiring additional processes. As a result, a process yield and reliability of the device are improved.

As the present invention may be embodied in several forms without departing from the spirit or essential characteristics thereof, it should also be understood that the above-described embodiments are not limited by any of the details of the foregoing description, unless otherwise specified, but

rather should be construed broadly within its spirit and scope as defined in the appended claims, and therefore all changes and modifications that fall within the meets and bounds of the claims, or equivalences of such meets and bounds are therefore intended to be embraced by the appended claims.

What is claimed:

1. A method for fabricating a semiconductor device comprising:

forming a field oxide layer defining an active region on a semiconductor substrate, the active region including a core device region and an input/output device region;

forming a thin gate oxide layer on the core device region and a thick gate oxide layer on the input/output device region;

forming gate electrodes on the gate oxide layers;

forming a first LDD region by ion-implanting low concentration impurity ions to the core device and input/output device regions of the active region;

forming a photoresist film pattern which is an LDD ion-implant mask for the input/output region, wherein the photoresist film exposes a portion of the semiconductor substrate at both sides of the gate electrode in the input/output device region and a portion of the semiconductor substrate adjacent to the field oxide layer at the outer rim of the core device region of the active region;

forming a second LDD region deeper than the first LDD region by implanting low concentration impurity ions by using the photoresist film pattern as an ion implant mask;

removing the photoresist film pattern;

forming an insulating film spacer on side walls of the gate electrodes;

forming a deep source/drain region and a shallow source/drain region by implanting high concentration impurity ions to the active region of the semiconductor substrate at least once, by using the insulating film spacer as an ion implant mask; and

forming a silicide film on the gate electrodes and the deep and shallow source/drain regions.

2. The method according to claim 1, wherein the low concentration impurity ion is As or P when the input/output device region and the core device region are defined as an NMOS region.

3. The method according to claim 1, wherein the low concentration impurity ion is BF_2, B_{11}, or In when the input/output device region and the core device region are defined as a PMOS region.

4. The method according to claim 1, wherein the high concentration impurity ion to form a deep source/drain region and a shallow source/drain region is As, P or combinations thereof when the input/output device region and the core device region are formed in an NMOS region.

5. The method according to claim 1, wherein the high concentration impurity ion is BF_2, B_{11}, In or combinations thereof, to form the deep source/drain region and the shallow source/drain region when the input/output device region and the core device region are defined as a PMOS region.

6. The method according to claim 1, wherein the ion implant process for forming the first LDD region is performed at a dose ranging from about 1×10^{13} to about 2×10^{15} ions/cm^2 with an ion implant energy ranging from about 10 to about 50 keV.

7. The method according to claim 1, wherein the ion implant process for forming the second LDD region is performed at a dose ranging from about 1×10^{13} to about 1×10^{15} ions/cm^2 with an ion implant energy ranging from about 10 to about 70 keV.

8. The method according to claim 1, wherein the second LDD region of the core device region is formed before the first LDD region is formed.

9. A method for fabricating a semiconductor device comprising:

forming a field oxide on a semiconductor substrate defining an active region, the active region having a core device region and an input/output device region, the input/output device region being disposed between the core device region and an inner rim of the field oxide;

forming a gate oxide layer on the core device region;

forming a gate electrode on the gate oxide layer;

forming a photoresist film pattern over the gate electrode and covering a portion of the input/output device region but leaving a portion of the input/output region exposed that extends from the inner rim of the field oxide to a point of the input/output device region spaced a predetermined distance from the gate electrode;

forming a first LDD region by ion-implanting low concentration impurity ions to the exposed input/output device region using the photoresist film patter as an ion implant mask;

removing the photoresist film pattern;

forming a second LDD region shallower than the first LDD region by implanting low concentration impurity ions and using gate electrode as an ion implant mask;

forming an insulating film spacer on side walls of the gate electrode;

forming a deep source/drain region and a shallow source/drain region by implanting high concentration impurity ions to the input/output device region at least once, using the insulating film spacer as an ion implant mask; and

forming a silicide film on the gate electrode and the deep and shallow source/drain regions.

10. The method according to claim 9, wherein the low concentration impurity ion is As or P when the input/output device region and the core device region are defined as an NMOS region.

11. The method according to claim 9, wherein the low concentration impurity ion is BF_2, B_{11}, or In when the input/output device region and the core device region are defined as a PMOS region.

12. The method according to claim 9, wherein the high concentration impurity ion to form a deep source/drain region and a shallow source/drain region is As, P or combinations thereof when the input/output device region and the core device region are formed in an NMOS region.

13. The method according to claim 9, wherein the high concentration impurity ion is BF_2, B_{11} In or combinations thereof, to form the deep source/drain region and the shallow source/drain region when the input/output device region and the core device region are defined as a PMOS region.

14. The method according to claim 9, wherein the ion implant process for forming the first LDD region is performed at a dose ranging from about $1\times10_{13}$ to about 2×10^{15} ions/cm^2 with an ion implant energy ranging from about 10 to about 50 keV.

15. The method according to claim 9, wherein the ion implant process for forming the second LDD region is performed at a dose ranging from about 1×10^{13} to about 1×10^{15} ions/cm^2 with an ion implant energy ranging from about 10 to about 70 keV.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,586,306 B2 Page 1 of 1
DATED : July 1, 2003
INVENTOR(S) : Bi Deuk Lee et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 6,
Line 22, delete "patter" and insert -- pattern --.
Line 38, delete "to." and insert -- to --.
Line 52, delete B11 In" and insert -- B11, In --.
Line 58, delete "1 x 10_{13}" and insert -- 1 x 10^{13} --.

Signed and Sealed this

Eleventh Day of November, 2003

JAMES E. ROGAN
Director of the United States Patent and Trademark Office

US006124172A

United States Patent [19]

Gardner et al.

[11] **Patent Number: 6,124,172**

[45] **Date of Patent: Sep. 26, 2000**

[54] **METHOD OF MAKING A SEMICONDUCTOR DEVICE HAVING SOURCE/DRAIN STRUCTURES WITH SELF-ALIGNED HEAVILY-DOPED AND LIGHTLY-DOPED REGIONS**

[75] Inventors: **Mark I. Gardner**, Cedar Creek; **Mark C. Gilmer**, Austin, both of Tex.

[73] Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, Calif.

[21] Appl. No.: **09/163,688**

[22] Filed: **Sep. 30, 1998**

[51] **Int. Cl.**[7] **H01L 21/331**; H01L 21/335; H01L 21/336

[52] **U.S. Cl.** **438/301**; 438/514; 438/526; 438/531; 438/532; 257/288; 257/336; 257/344; 257/408

[58] **Field of Search** 438/305, 303, 438/301, 304; 257/388, 336, 344

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,818,715	4/1989	Chao	438/303
4,907,048	3/1990	Huang	357/23.9
5,061,647	10/1991	Roth et al.	438/304
5,256,586	10/1993	Choi et al.	438/304
5,276,347	1/1994	Wei et al.	257/388
5,726,479	3/1998	Matsumoto et al.	257/412
5,863,837	1/1999	Sudo	438/692

OTHER PUBLICATIONS

Wolf, *Silicon Processing for the VLSI Era*, Lattice Press, vol. 2; Process Integration, pp. 354--363 (1960).

S. Wolf, "Silicon Processing for the VLSI Era", vol. 2, Lattice Press, CA, USA, 1990.

Primary Examiner—Tom Thomas
Assistant Examiner—Bernard E. Souw

[57] **ABSTRACT**

A method of making a semiconductor device includes forming gate electrode over a substrate and a protective layer over the gate electrode. A portion of the protective layer is selectively removed to expose a peripheral region of the gate electrode. A remainder of the protective layer remains disposed over a central region of the gate electrode. An upper portion of the peripheral region of the gate electrode is then removed typically leaving an underlying portion. Often, a dopant material is implanted into the substrate adjacent to and beneath the underlying portion to simultaneously form lightly-doped and heavily-doped regions beneath and adjacent to the underlying portion, respectively. In addition, all or part of the underlying portion may be oxidized to provide a gate electrode with reduced width.

27 Claims, 5 Drawing Sheets

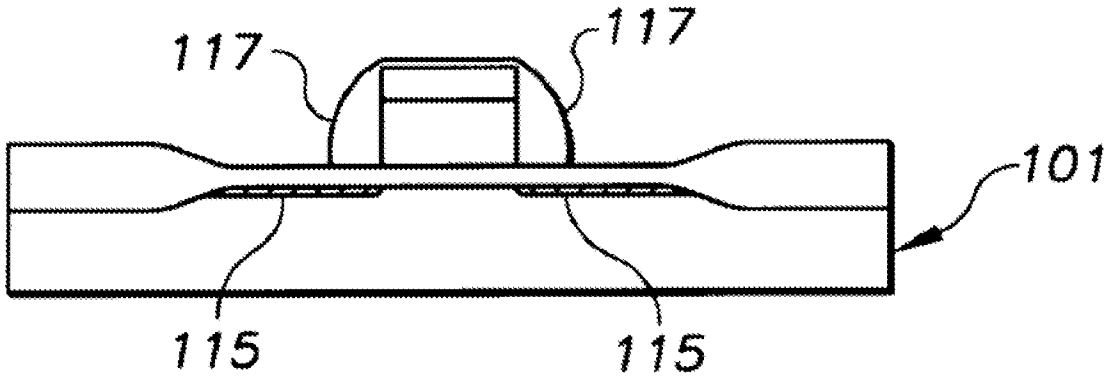


FIG. 1A

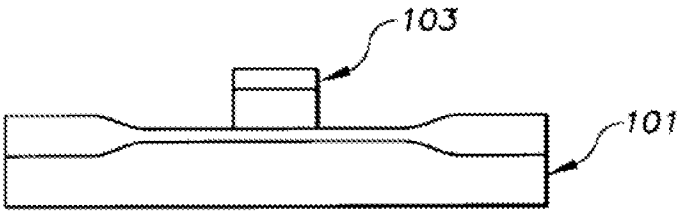


FIG. 1B

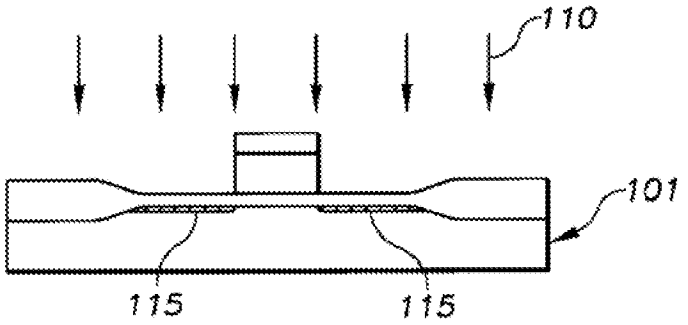


FIG. 1C

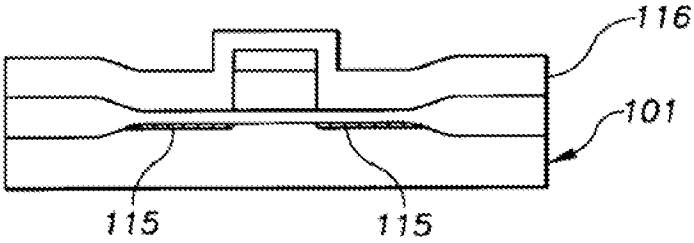


FIG. 1D

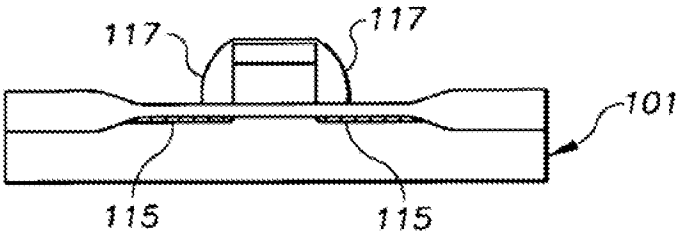


FIG. 1E

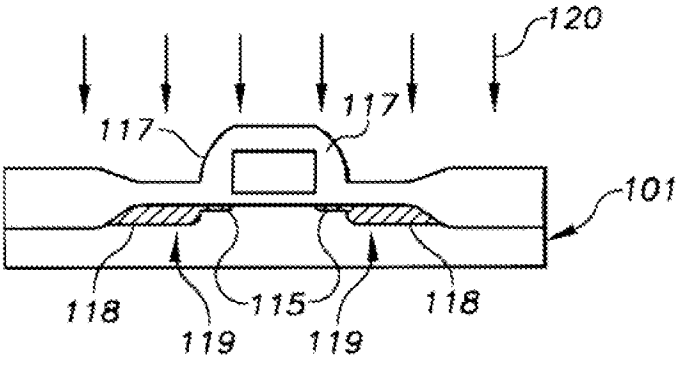


FIG. 2A

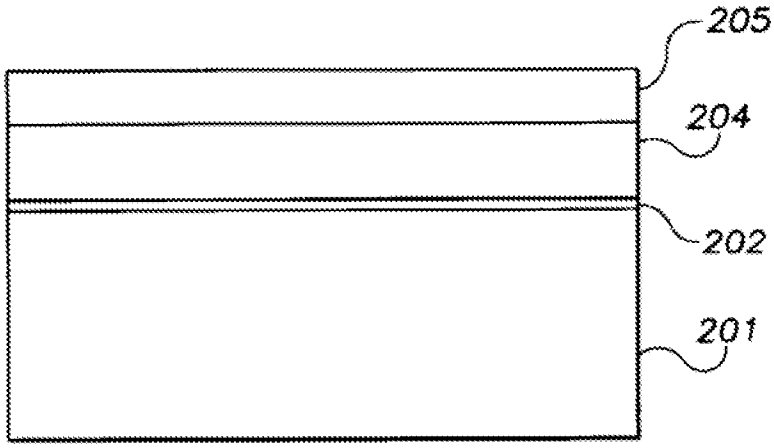


FIG. 2B

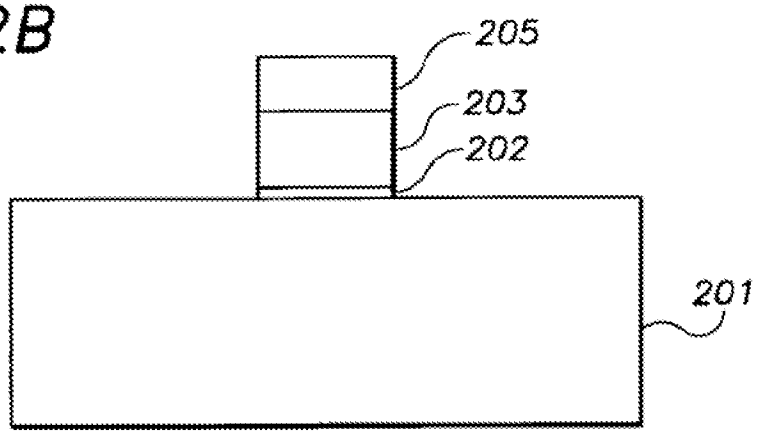


FIG. 2C

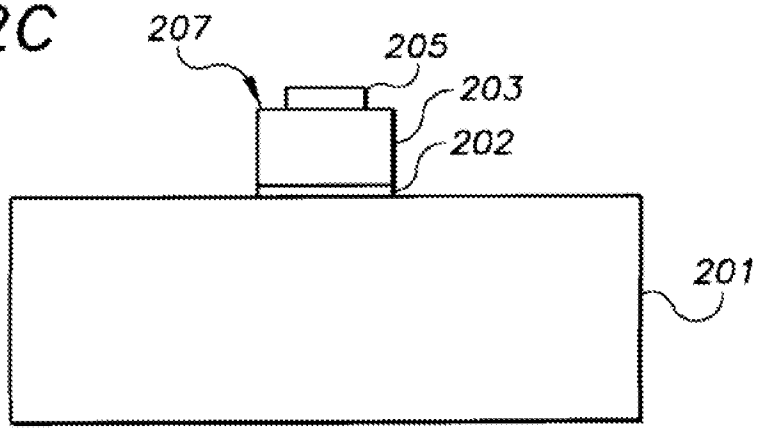


FIG. 2D

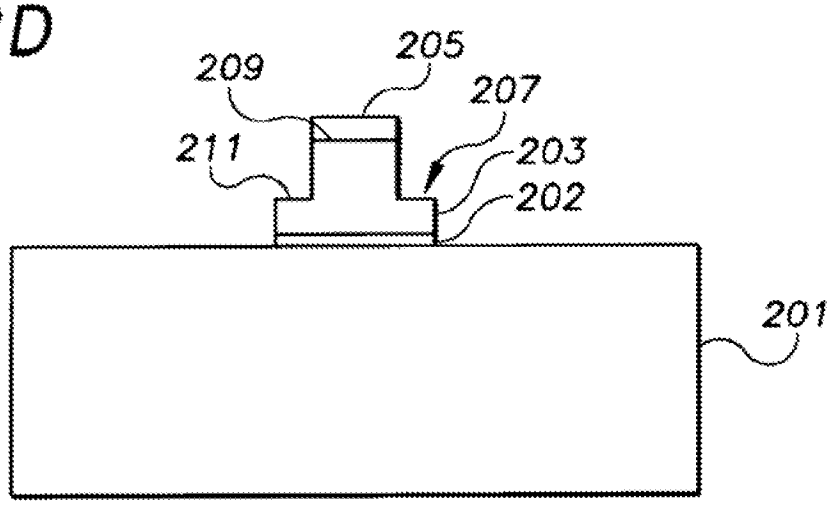

209
205
207
211
203
202
201

FIG. 2E

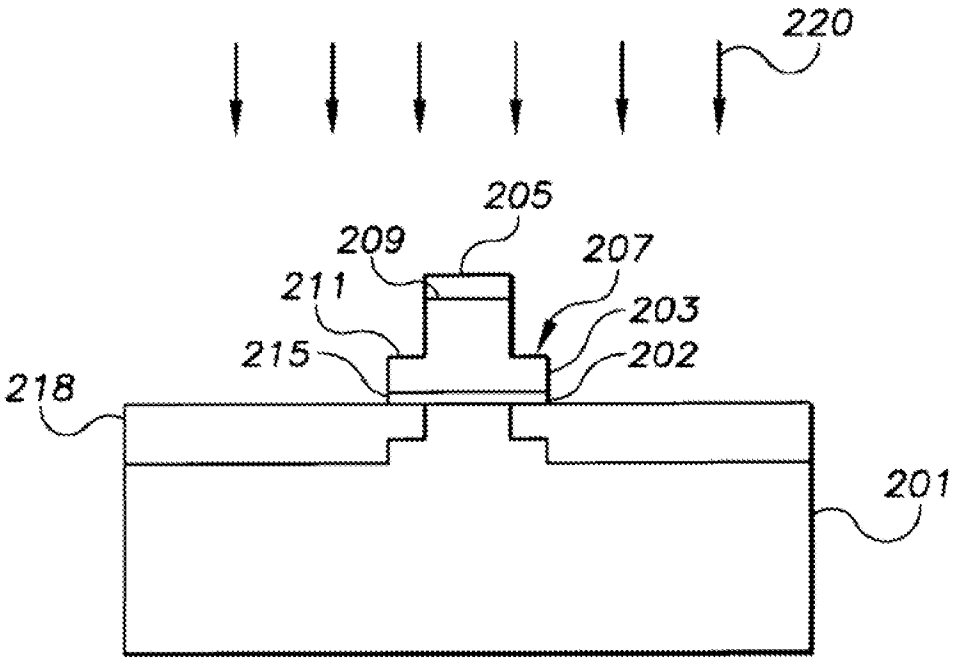

220
205
209
207
211
203
215
202
218
201

FIG. 3A

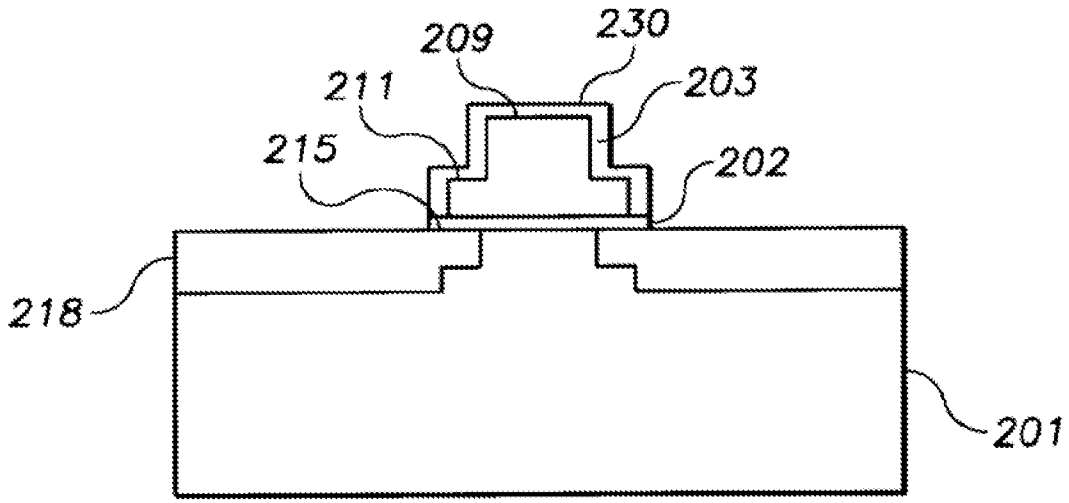


FIG. 3B

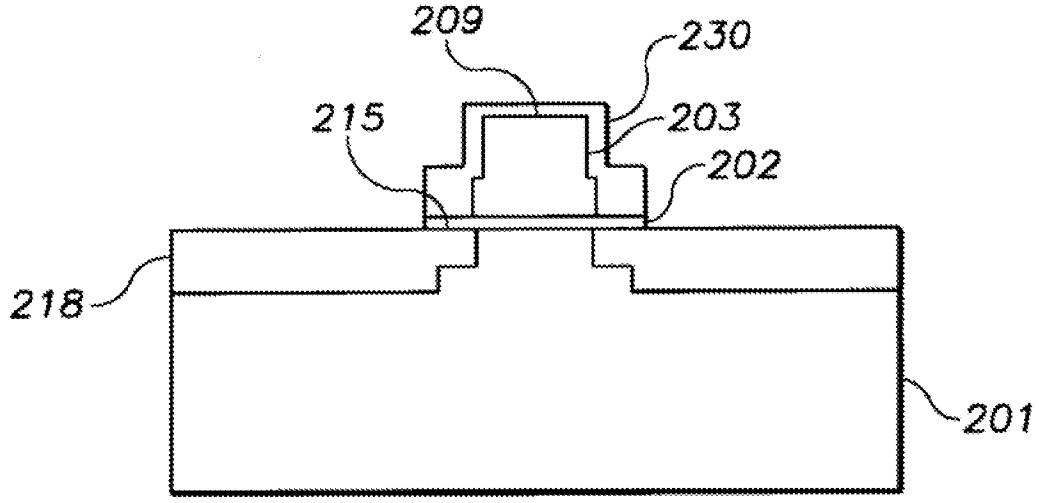


FIG. 4A

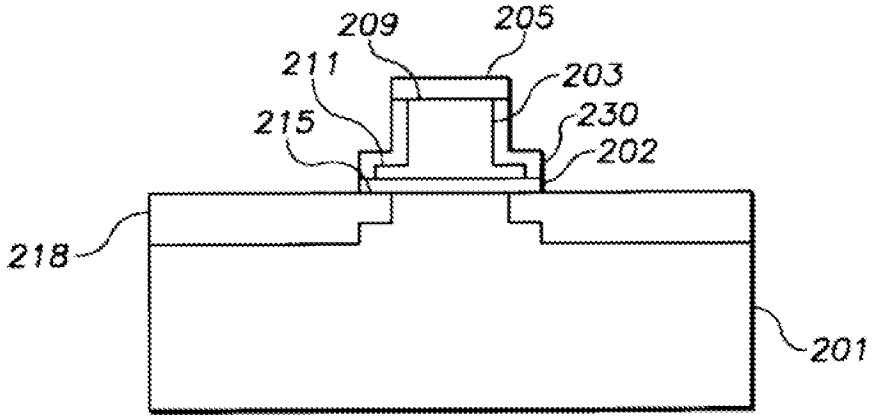


FIG. 4B

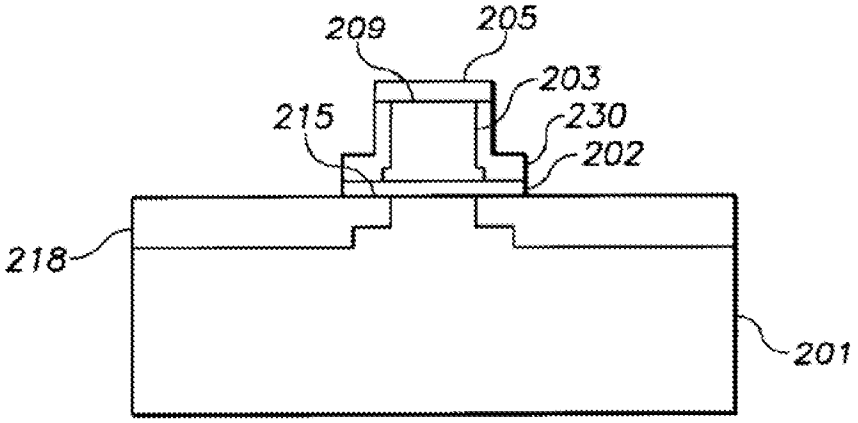
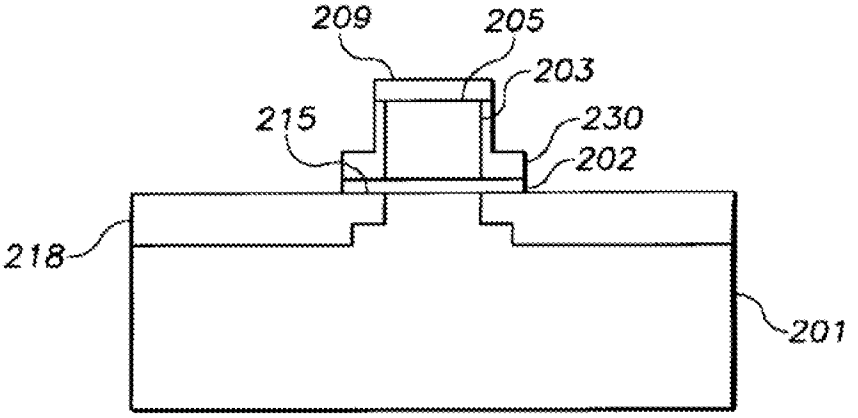


FIG. 5



METHOD OF MAKING A SEMICONDUCTOR DEVICE HAVING SOURCE/DRAIN STRUCTURES WITH SELF-ALIGNED HEAVILY-DOPED AND LIGHTLY-DOPED REGIONS

FIELD OF THE INVENTION

The present invention is, in general, directed to a semiconductor device and a method of manufacture thereof. More particularly, the present invention relates to methods of making a semiconductor device having source/drain structures with self-aligned heavily-doped and lightly-doped regions and/or a narrow gate electrode.

BACKGROUND OF THE INVENTION

Over the last few decades, the electronics industry has undergone a revolution by the use of semiconductor technology to fabricate small, highly integrated electronic devices. The most common semiconductor technology presently used is silicon-based. A large variety of semiconductor devices have been manufactured having various applications in numerous disciplines. One such silicon-based semiconductor device is a metal-oxide-semiconductor (MOS) transistor. The MOS transistor is used as one of the basic building blocks of most modern electronic circuits. Thus, such circuits realize improved performance and lower costs as the performance of the MOS transistor is increased and as the manufacturing costs are reduced.

A typical MOS semiconductor device generally includes a semiconductor substrate on which a gate electrode is disposed. The gate electrode, which acts as a conductor, receives an input signal to control operation of the device. Source and drain regions are typically formed in regions of the substrate adjacent to the gate electrodes by heavily doping the regions with a dopant material of a desired conductivity. The conductivity of the doped region depends on the type and concentration of the impurity used to dope the region. The typical MOS transistor is symmetrical, which means that the source and drain are interchangeable. Whether a region acts as a source or drain typically depends on the respective applied voltages and the type of device being made. The collective term source/drain region is used herein to generally describe an active region used for the formation of either a source or drain.

A channel region is formed in the semiconductor substrate beneath the gate electrode and between the source and drain regions. The channel is typically lightly-doped with a dopant material. The gate electrode is generally separated from the substrate by an insulating layer, typically an oxide layer such as SiO_2. The insulating layer is provided to prevent current from flowing between the gate electrode and the source, drain or channel regions. In operation, a voltage is typically developed between the source and drain terminals. When an input voltage is applied to the gate electrode, a transverse electric field is set up in the channel region. By varying the transverse electric field, it is possible to modulate the conductance of the channel region between the source and drain regions. In this manner, an electric field is used to control the current flow through the channel region. This type of device is commonly referred to as a MOS field-effect-transistor (MOSFET).

MOS devices typically fall in one of two groups depending on the type of dopant materials used to form the source, drain and channel regions. The two groups are often referred to as n-channel and p-channel devices. The type of channel is identified based on the conductivity type of the channel which is developed under the transverse electric field. In an n-channel MOS (NMOS) device, for example, the conductivity of the channel under a transverse electric field is of the conductivity type associated with n-type impurities (e.g., arsenic or phosphorous). Conversely, the channel of a p-channel MOS (PMOS) device under the transverse electric field is associated with p-type impurities (e.g., boron).

A number of different techniques and fabrication processes may be used to form MOS devices. With reference to FIGS. 1A-1E, one typical MOS fabrication process is depicted to form semiconductor structures with source/drain structures having heavily-doped regions and adjacent lightly-doped regions commonly referred to as lightly-doped rain (LDD) regions. LDD structures are often used in the formation of semiconductor devices having short channels to prevent or reduce short-channel effects.

As depicted in FIG. 1A, a gate electrode **103** is formed on a substrate **101**. An LDD region **115** is formed in the substrate **101** by implanting a relatively low dose of a dopant material **110** into the exposed areas, as illustrated in FIG. 1B. Following the LDD implant, a spacer layer **116** is formed and etched to form spacers **117** on sidewalls of the gate electrode **103**, as illustrated in FIGS. 1C and 1D. The substrate **101** is again implanted with a heavy dose of dopant material **120** aligned with the spacers **117** to form heavily-doped regions **118**, which together with the LDD regions **115**, form LDD source/drain structures **119**, as illustrated in FIG. 1E. Following formation of the LDD structures **119**, further processing such as silicidation and interconnect formation is performed. A more detailed description of the elements and fabrication of source/drain structures may be found in S. Wolf, *Silicon Processing for the VLSI Era*, Vol. 2: Processing Integration, pp. 354–363.

Semiconductor devices, like the one described above, are used in large numbers to construct most modern electronic devices. In order to increase the capability of such electronic devices, it is necessary to integrate even larger numbers of such devices into a single silicon wafer. As the semiconductor devices are scaled down (i.e., made smaller) to form a larger number of devices on a given surface area, the structure of the devices and fabrication techniques used to make such devices must be altered.

The above described conventional techniques for forming MOS devices impose limitations on the minimum gate width and on the proper alignment of the independently-formed lightly-doped and heavily-doped regions of the source/drain structures. For example the minimum width of the gate electrode presently depends on the resolution of the photolithographic techniques employed. Thus, there is a need for new methods for forming narrower gate electrodes, including methods that are not limited by photolithographic resolution.

Moreover, as the size of semiconductor devices decreases, it becomes critical to ensure that structures, such as lightly-doped and heavily-doped regions in source/drain structures, are properly aligned with each other and with other structures of the device, such as the gate electrode. Thus, there is a need for methods of manufacture that provide accurate alignment of these structures.

SUMMARY OF THE INVENTION

Generally, the present invention relates to a variety of techniques for forming a semiconductor device having self-aligned heavily-doped and lightly-doped regions and/or a narrower gate. One embodiment of the invention is a method for making a semiconductor device. A gate electrode is

formed over a substrate and a protective layer is formed over the gate electrode. Next a portion of the protective layer is selectively removed to expose a peripheral region of the gate electrode. A remainder of the protective layer remains disposed over a central region of the gate electrode. An upper portion of the peripheral region of the gate electrode is then removed typically leaving an underlying portion. A dopant material may be implanted into the substrate adjacent to and beneath the underlying portion. Often, lightly-doped and heavily-doped regions are simultaneously formed beneath and adjacent to the underlying portion of the peripheral region of the gate electrode, respectively, during this implantation process. In addition or alternatively, all or part of the underlying portion may be oxidized to provide a gate electrode with reduced width.

Another embodiment of the invention is a semiconductor device having a substrate and a gate electrode disposed over the substrate. The gate electrode has a central region with a first thickness and a peripheral region extending laterally from the central region with a second thickness that is less than the first thickness.

The above summary of the present invention is not intended to describe each disclosed embodiment or every implementation of the present invention. The Figures and the detailed description which follow more particularly exemplify these embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be more completely understood in consideration of the following detailed description of various embodiments of the invention in connection with the accompanying drawings, in which:

FIGS. **1A** through **1E** illustrate a conventional process for forming a semiconductor device;

FIGS. **2A** through **2E** illustrate an exemplary fabrication process for forming a device in accordance with one embodiment of the invention;

FIG. **3A** through **3B** illustrate two exemplary semiconductor device structures formed in accordance with embodiments of the invention;

FIGS. **4A** through **4B** illustrate another two exemplary semiconductor device structures formed in accordance with yet other embodiments of the invention; and

FIG. **5** illustrates yet another exemplary semiconductor device structure formed in accordance with another embodiment of the invention.

While the invention is amenable to various modifications and alternative forms, specifics thereof have been shown by way of example in the drawings and will be described in detail. It should be understood, however, that the intention is not to limit the invention to the particular embodiments described. On the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE DRAWINGS

The present invention is believed to be applicable to a number of semiconductor devices using gate electrodes. Such semiconductor devices may include NMOS, CMOS, PMOS and BiCMOS devices for example. The invention has been found to be particularly advantageous in application environments where it is desirable to form source/drain structures having lightly-doped drain (LDD) regions and/or to form a narrow gate electrode in a MOS device. While the present invention is not so limited, an appreciation of various aspects of the invention is best gained through a discussion of various application examples of processes used to form such semiconductor devices.

FIGS. **2A** through **2E** illustrate an exemplary process for fabricating a semiconductor device in accordance with one embodiment of the invention. A gate electrode layer **204** is formed on a substrate **201** as illustrated in FIG. **2A**. The gate electrode layer **204** is typically insulated from the substrate **201** by a gate insulating layer **202**. The gate insulating layer **202** is often formed using an oxide material, such as silicon dioxide. Other materials, however, may be used, including, for example, silicon nitride, silicon oxynitride, nitrided silicon oxide (SiO_xN_y), and other oxides, such as metal oxides. The gate insulating layer **202** may be formed by a variety of techniques, including, for example, chemical vapor deposition, physical vapor deposition, spin-on glass formation, and thermal oxidation of the substrate.

The gate electrode layer **204** may be formed using a variety of materials including, for example, polysilicon and metals, such as, for example, aluminum, tungsten, copper, iridium, titanium and cobalt. Typically, the gate electrode layer **204** is made of polysilicon. The gate electrode layer **204** may be formed using a variety of techniques, including, for example, chemical vapor deposition, physical vapor deposition, and sputtering.

A protective layer **205** is formed over a top surface of the gate electrode layer **204**, as shown in FIG. **2A**. The material used to form the protective layer **205** is typically a dielectric material, however, other materials may be used. The protective layer **205** is often formed using a material that can be selectivity etched with respect to the gate electrode layer. Examples of suitable materials include, for example, silicon nitride, silicon oxynitride, nitrided silicon oxide, silicon dioxide, or materials that form an antireflective coating over the gate electrode layer **204**. The protective layer **205** may be formed using a variety of techniques, including, for example, chemical vapor deposition, physical vapor deposition, sputtering, and spin-on glass formation.

A gate electrode **203** is then formed including removal of portions of the gate electrode layer **204**, gate insulating layer **202**, and protective layer **205**, as shown in FIG. **2B**. This can be accomplished, for example, by depositing photoresist material over the protective layer and then patterning and etching to leave photoresist material over only those regions corresponding to the gate electrode(s). The exposed protective layer and underlying gate electrode layer can be simultaneously or sequentially removed by techniques, such as, for example, selective and/or anisotropic etching. Portions of the gate insulating layer **202** adjacent to the gate electrode **203** may be removed, as shown, or kept, if desired. Typically, the gate electrode **203** has an initial width ranging from, for example, 1500 to 3500 Angstroms (0.15 to 0.35 μm) when formed, however, this process can also be used with smaller or larger gate electrodes.

Other processes can also be used to form the gate electrode **203** and protective layer **205** structure depicted in FIG. **2B**. In one alternative embodiment, photoresist material (not shown) is deposited on the substrate, patterned, and etched to form openings (not shown) exposing a portion of the substrate and corresponding to the position of the gate electrodes. An insulating layer is formed on the substrate within the opening by chemical vapor deposition, physical vapor deposition, or thermal oxidation. The gate electrode is then formed in the opening using known deposition and polishing techniques. The protective layer is formed in the

opening above the gate electrode. The protective layer may also be formed using known deposition and polishing techniques. The remaining photoresist material may then be removed leaving the gate electrode and protective layer.

Returning to FIGS. 2A-2E, the protective layer **205** initially extends over the entire gate electrode **203**. After formation, the protective layer **205** is selectively trimmed, as illustrated in FIG. 2C. Selectively trimming the protective layer **205** exposes and defines a peripheral region **207** of the gate electrode **203**. The remaining portion of the protective layer **205** is disposed over and defines a central region **209** of the gate electrode **203**. The selective trimming can be accomplished by a number of techniques, including, for example, selectively and/or isotropically or anisotropically etching the protective layer **205**. Often, the etching of the protective layer **205** is a timed etching process to achieve a desired amount of exposure of the peripheral region of the gate electrode **203**.

A lower portion of the peripheral region will be used to form LDD regions. The width of the peripheral region and the amount of trim is suitably selected in consideration of the desired width of the LDD regions. The amount of trim may range from, for example, about 250 to 500 Angstroms, although larger or smaller peripheral regions can be exposed. Depending on the initial width of the gate, this trimming process can be used to reduce the size of the gate electrode by 5 to 50% or more.

Typically, isotropic etching removes portions of both the top and sides of the protective layer **205**. Often isotropic etching reduces the thickness of the protective layer by an amount equal to the amount that is etched away from each side of the protective layer **205**. Thus, when using an isotropic etch, the initial thickness of the protective layer **205** is usually provided to be larger (typically at least 20% larger) than the distance that the protective layer **205** is etched back from the peripheral edge of the gate electrode **203**.

Anisotropic etching can also be used. Anisotropic etching typically results in the top surface of the protective layer **205** being etched faster or slower than the sidewalls. The thickness of the protective layer **205** is typically appropriately sized to leave a portion of the protective layer **205** after etching.

For many applications, the initial thickness of the protective layer **205** is typically at least 300 Angstroms and, usually, at least 600 Angstroms. Often the initial thickness of the protective layer **205** ranges from, for example, 1000 to 3000 Angstroms. Usually the protective layer **205** has a thickness of at least 50 Angstroms and often at least 500 to 1000 Angstroms after exposing the peripheral region **207** of the gate electrode **203**.

After the peripheral region **207** is exposed, an upper portion of the peripheral region **207** of the gate electrode **203** can be removed to typically leave an underlying portion **211**, as shown in FIG. 2D. The protective layer **205** usually prevents the removal of any substantial portion of the central region **209** of the gate electrode **203**. The removal of the upper portion of the peripheral region **207** can be accomplished by a variety of techniques, including, for example, anisotropic etching techniques. Often, an anisotropic etching technique is used so that the width of the gate electrode **203**, at its base near the substrate **201**, is not reduced at all or is only reduced by a relatively small amount. The etchants used to remove the upper portion of the peripheral region **207** of the gate electrode **203** may or may not be selective to the gate electrode **203**. If the gate electrode **203** is not selectively etched, then the thickness of the protective layer **205** is typically large enough to prevent etching of the underlying central region **209** of the gate electrode **203**.

By removing the upper portion of the peripheral region **207**, the thickness of the gate electrode **203** in the peripheral region **207** is reduced. Typically, the thickness of the underlying portion **211** of the peripheral region **207** ranges from, for example, 100 to 500 Angstroms, although larger or smaller underlying portions of the peripheral region **207** may be formed. The thickness of the underlying portion of the peripheral region **207** may determine, at least in part, the depth of a lightly-doped region **215** (see FIG. 2E).

The amount of the reduction in thickness of the peripheral region **207** can be controlled by a variety of techniques, including, for example, using timed etching to remove only a desired amount of material or using an etch stop. One suitable etch stop is a nitrogen-bearing region within the gate electrode **203**. The nitrogen-bearing region may be formed by implantation of a nitrogen species into the gate electrode or by forming a lower portion of the gate electrode layer **204** in a nitrogen-bearing ambient. In addition to providing an etch stop, the nitrogen in the lower portion of the gate electrode may be advantageous because nitrogen can often prevent or reduce penetration of dopant material, such as boron, from the channel during formation or operation of the semiconductor device.

A dopant material **220** is implanted into the substrate **201** to simultaneously form heavily-doped regions **218** and lightly-doped regions **215**, as shown in FIG. 2E. The lightly-doped regions **215** and the heavily-doped regions **218** may be used as source/drain regions in the ultimately formed device. This single dopant implant step results in self-alignment of the lightly-doped regions **215** and heavily-doped regions **218** of the source and drain structures. This self-alignment of the heavily-doped regions **218** and lightly-doped regions **215** may reduce alignment errors between these regions and improve the reliability of the device.

Suitable n-type dopant materials include, for example, arsenic (As) and phosphorus (P). Suitable p-type dopant materials include, for example, boron and boron compounds, such as boron hydride and boron halides. Other suitable p-type dopant materials include, for example, indium and gallium. The implant energies and dosages of this implant are typically selected to provide a desired depth and resistivity of the lightly-doped regions **215** and heavily-doped regions **218**. For many applications, suitable implant energies and dosages of the dopant material **220** range from, for example, 5 to 50 keV and 2E15 (2×10^{15}) to 8E15 (8×10^{15}) dopant atoms/cm^2, respectively. An optional anneal may be performed after implantation to activate the dopant material.

The protective layer **205** can be removed either before or subsequent to the implantation of the dopant material. The removal of the protective layer **205** can be performed by a variety of techniques, including, for example, selective etching and chemical, mechanical, or chemical/mechanical polishing.

Spacers may be formed on sidewalls of the gate electrode to prepare the device for silicidation. The spacers may be formed using conventional deposition and etching techniques. Alternatively, sidewall spacers may be formed by oxidizing the gate electrode. For example, the underlying portion **211** of the peripheral region **207** of the gate electrode **203** can be partially oxidized to form an optional oxide layer **230** that can be used as a spacer, as shown in FIG. 3A. Partial oxidation results in a gate electrode **203** with peripheral

portions **207** extending from a thicker central region **209**. The portion of the oxide layer **230** over the top of the gate electrode **203** may be removed by known techniques, such as, for example, anisotropic etching, prior to silicidation.

In other embodiments, the underlying portion **211** of the peripheral region **207** may be completely oxidized (i.e., substantially all of the original underlying portion **211** is oxidized) to form an oxide layer **230**, as shown in FIG. **3B**. The gate electrode **203** in these embodiments can have a width that is greatly reduced from the initial width. Although this can result in a gate electrode **203** having substantially straight sidewalls, in at least some instances, the gate electrode **203** may have slight extensions and/or sloped sidewalls. The lightly-doped regions **215** may extend to the reduced gate electrode **203** as a result of thermal diffusion after an annealing process.

In yet other embodiments, the protective layer **205** is not removed before the formation of the optional oxide layer **230** by either partial or complete oxidation, as shown in FIGS. **4A** and **4B**, respectively. The use of the protective layer **205** to protect the upper surface of the central portion **209** of the gate electrode **203** from oxidation can prevent or restrict the formation of an unwanted oxide layer over the central portion **209** of the gate electrode **203**. The protective layer **205** may be removed and the upper surface of the gate electrode can then be used, for example, to form a silicide contact by known silicidation techniques.

In another embodiment, oxidation of the underlying portion **211** of the gate electrode **203** is performed at a faster rate than the oxidation of the central region **209** of the gate electrode to form the structure illustrated in FIG. **5**. This can be accomplished by, for example, leaving the protective layer **205** over the central region **209** of the gate electrode **203** during the implantation of an n-type dopant material **220**. Thermal oxidation of the gate electrode occurs more rapidly in n-doped polysilicon than in undoped polysilicon. Thus, the peripheral region **207** of the gate electrode **203** may be more rapidly oxidized than the central region **209**.

The above process can be used to form a number of different semiconductor devices, including, but not limited to, MOS structures such as PMOS devices, NMOS devices, complimentary MOS (CMOS) semiconductor devices having both PMOS and NMOS devices and bipolar CMOS (BiCMOS) devices. In a CMOS device, for example, the NMOS device regions may be masked off while the above process is carried out on the PMOS device regions and the PMOS device regions may be masked off while the above process is carried out on the NMOS device regions. Alternatively, fabrication of the NMOS and PMOS device regions may occur simultaneously, with masking typically used only during the dopant implantation steps. For example, during the dopant implantation of the device regions of the NMOS region, the PMOS region is masked, and vice versa. Fabrication may continue with well-known processing steps including, for example, silicidation, interconnect formation and so forth to complete the ultimate device structure.

As noted above, the present invention is applicable to the fabrication of a number of semiconductor devices, including in particular MOS structures, having source/drain regions and LDD regions or a narrower gate electrode. Accordingly, the present invention should not be considered limited to the particular examples described above, but rather should be understood to cover all aspects of the invention as fairly set out in the accompanying claims. Various modifications, equivalent processes, as well as numerous structures to which the present invention may be applicable will be readily apparent to those of skill in the art to which the present invention is directed upon review of the present specification. The claims are intended to cover such modifications and devices.

What is claimed is:

1. A method for making a semiconductor device, comprising:

forming a gate electrode over a substrate including one of implanting a nitrogen species into a lower portion of the gate and forming a lower portion of the gate electrode in a nitrogen-bearing ambient, the lower portion having a nitrogen-bearing region adapted to act as an etch stop;

forming a protective layer over the gate electrode;

selectively removing a portion of the protective layer to expose a peripheral region of the gate electrode, a remainder of the protective layer remaining disposed over a central region of the gate electrode, and

using the etch stop and removing an upper portion of the peripheral region of the gate electrode.

2. The method of claim **1**, wherein removing the upper portion of the peripheral region of the gate electrode comprises leaving a lower portion of the peripheral region.

3. The method of claim **2**, further comprising oxidizing a part of the underlying portion.

4. The method of claim **3**, further comprising implanting a dopant material in the substrate to simultaneously form a lightly-doped region beneath the underlying portion of the peripheral region of the gate electrode and a heavily-doped region adjacent to the gate electrode subsequent to oxidizing a part of the underlying portion.

5. The method of claim **3**, further comprising implanting a dopant material in the substrate to simultaneously form a lightly-doped region beneath the underlying portion of the peripheral region of the gate electrode and a heavily-doped region adjacent to the gate electrode prior to oxidizing a part of the underlying portion.

6. The method of claim **3**, wherein oxidizing a part of the underlying portion includes oxidizing substantially all of the underlying portion.

7. The method of claim **2**, further comprising implanting a dopant material in the substrate to simultaneously form a lightly-doped region beneath the underlying portion of the peripheral region of the gate electrode and a heavily-doped region adjacent to the gate electrode.

8. The method of claim **1**, wherein selectively removing a portion of the protective layer to expose a peripheral region comprises selectively removing a portion of the protective layer to expose a peripheral region extending inward from an edge of the gate electrode up to 500 Angstroms.

9. The method of claim **1**, further comprising removing the protective layer.

10. The method of claim **9**, wherein the protective layer is removed prior to implanting the dopant material.

11. The method of claim **9**, wherein the protective layer is removed subsequent to implanting the dopant material.

12. The method of claim **9**, further comprising oxidizing, prior to removing the protective layer, at least a part of an underlying portion of the gate electrode remaining after removal of the upper portion of the peripheral region of the gate electrode.

13. The method of claim **9**, further comprising oxidizing, subsequent to removing the protective layer, at least a part of an underlying portion of the gate electrode remaining after removal of the upper portion of the peripheral region of the gate electrode.

14. A method for making a semiconductor device, comprising:

forming a gate electrode over a substrate including one of implanting a nitrogen species into a lower portion of the gate and forming a lower portion of the gate electrode in a nitrogen-bearing ambient, the lower portion having a nitrogen-bearing region adapted to act as an etch stop;

forming a protective layer over the gate electrode;

selectively removing a portion of the protective layer to expose a peripheral region of the gate electrode, a remainder of the protective layer remaining disposed over a central region of the gate electrode; and

using the etch stop and removing an upper portion of the peripheral region of the gate electrode leaving an underlying portion; and

forming simultaneously a heavily-doped region in the substrate adjacent the gate electrode and a lightly-doped region in the substrate beneath the underlying portion of the gate electrode.

15. The method of claim 14, further comprising oxidizing a part of the underlying portion.

16. The method of claim 14, further comprising oxidizing substantially all of the underlying portion.

17. The method of claim 14, wherein forming simultaneously the heavily-doped region in the substrate adjacent the gate electrode and the lightly-doped region in the substrate beneath the underlying portion of the peripheral region of the gate electrode comprises implanting a dopant material into the substrate.

18. A semiconductor device, comprising:

a substrate; and

a gate electrode disposed on the substrate, the gate electrode having a central region with a first thickness and a peripheral region extending laterally from the central region with a second thickness that is less than the first thickness, a lower portion of the peripheral region nearest the substrate having one of a nitrogen implant forming a nitrogen-bearing region and a lower portion of the gate electrode formed in a nitrogen-bearing ambient.

19. The semiconductor device of claim 18, wherein the gate electrode has a width ranging from 500 to 2000 Angstroms.

20. The semiconductor device of claim 18, wherein the central region of the gate electrode has a width ranging from 500 to 1500 Angstroms.

21. The semiconductor device of claim 18, further comprising a dielectric layer disposed on at least a portion of the gate electrode.

22. The semiconductor device of claim 21, wherein the dielectric layer comprises a thermally oxidized portion of the gate electrode.

23. A semiconductor device formed by the method of claim 1.

24. The method of claim 1, wherein forming a gate electrode over a substrate comprises:

forming a thin gate oxide layer on the substrate;

forming a gate electrode layer on the thin gate oxide layer;

forming a protective layer over the gate electrode layer;

patterning a mask layer on a selected portion of the protective layer; and

using the patterned mask layer and selectively removing portions of the protective layer, the gate electrode layer, and the thin gate oxide layer not patterned by the mask layer to expose the substrate.

25. The device of claim 18, wherein the nitrogen-bearing region is adapted to reduce penetration of dopant material from a channel in the substrate below the gate.

26. The device of claim 18, wherein the nitrogen-bearing region is adapted to prevent penetration of dopant material from a channel in the substrate below the gate.

27. The device of claim 18, wherein the nitrogen-bearing region is formed across the entire width of the gate.

* * * * *

RELATED PROCEEDINGS APPENDIX

None.